

Block Diagram



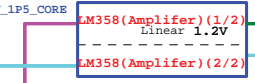
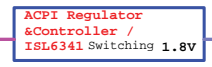
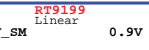
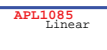
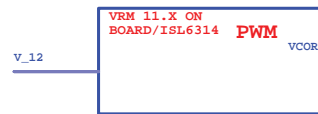
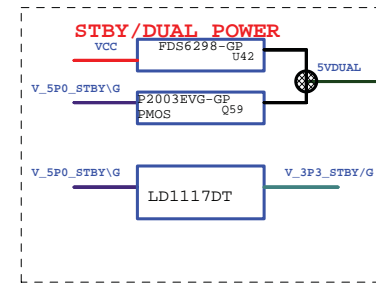
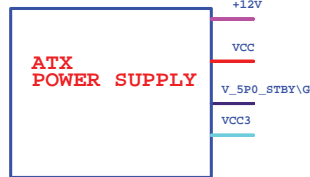
[Variant Name]		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
			
Title			
BLOCK DIAGRAM & PAGE INDEX			
Size	Document Number	Rev	
A2	S15	-1	
Date	Friday, December 12, 2008	Sheet	1 of 50

Rev. History

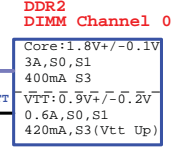
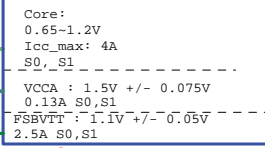
DATE	Rev	Description
0725	SA	Add C493-C509 for EMI solution
0729	SA	R152,R154-R160 change to Dummy on page 27 R8 change to 0 ohm on page 9 R10 change to 1.2K ohm on page 9 R52,R54 change to Dummy on page 19
0730	SA	change R69,R70,R71 to 150 Ohm on page 21 change R340,R342,R344 to 150 Ohm on page 41 R129 to 33 ohm on page 25 delete Net CK410_VDDPCI,and change to VDD_SRC_CLKA on page 25 change R146 to DUMMY on page25 delete TP48,TP49 and add R610,R611 on page 26 ADD R612,R613 on page 28 Change R392 value from 35.7k to 11k Add C8 to reduce noise on current sense amplifier Add R405(11.3KR) Add C345 (1000PF) Change R407 from 2.1K to 10KR Change C343 from 15nF to 820PF Change C341 from 180P to 100P Change R385 from 10k to 16.9kR Add R422 for power source filter Delete R592 and R579 Change R575 from 2.1K to 3KR Add C379, C387 (10uF) for V_SM Add C389 and C390 (10uF) for V_1P5_CORE Change R593 from 10KR to 12KR Change C477 from 4700pF to 10nF Change R596 from 18KR to 24KR Change R580 from 10KR to 15KR Change C468 form 4700pF to 10nF Change C583 from 18KR to 22KR Change R391 to 470R Delete TP122 and add R614, JP3 on page28 change R600 pin2 from net ICH_VRMPWRGD_PU to ICH_THRM_PU_N on page 38 R194,R195,R196 mount 8.2K on page 32 R529 change from 560K to 15K on page 35 R526 change from 560K to 15K on page 36 R347 change from 560K to 15K on page 36 Delete TP119 and TP120, chagne net TP119 and TP 120 to ICH_GPIO38 and ICH_GPIO39 and pull high to VCC3 on page28 delete R170 change to 10K on page 28 delete R287 delete C184 R176 change to Dummy,for VRM's power good already pull high change C439 & R475 power source from VCC to V_5P0_STBY\G on page 50 Add D4 for Intel Recommend R492,R495, C444change to Dummy Add R617 and connector to ICH_VRMPWRGD_PU
0731	SA	TC3,TC4,TC5-SE560U2D5VM-GP EOL change to SE560U2D5VM-1-GP ON PAGE44 change USBP8+,USBP8- to ICH7 port 7,change USB_FRONT1 and USB_FRONT2 to ICH port 4,5 ON PAGE26 delete net USB_OC4#_PULL_UP,USB_OC5#_PULL_UP,USB_OC_FRONT_67, CHANGE TO USB_OC6#_PULL_UP,USB_OC7#_PULL_UP,USB_OC_FRONT_12 ON PAGE26 IND-1UH-64-GP change to IND-1UH-41-GP-U ON PAGE 48 U25 AT24C08AN-1-GP EOL change to AT24C08BN-SH-T-GP ON PAGE35 Add R226 Dummy, and connector to ICH_GPIO12 ON PAGE 28 R604 change to Dummy on page 38 Add R618 pull high to V_3P3_STBY\G on page38 Add C510 on page38
0806	SA	Change the U14 power source from V_SM to VCC3 on page 45
0808	SA	Change JRI library,add L6,R623~R626
0811	SA	F6 ,F7 FUSE-1D5A6V-7GP EOL change to 69.50007.961 change the SMI321 write protect from ICH_GPIO14 to ICH_GPIO16,because of power plane issue Add R627 Add stitching caps C515,C516,C517,C518 change net RESET_BUTTON from SIO GP54 to ICH_GPIO10,Add SIO GP54 to TP138
0812	SA	delete R551(pull high to VCC3) add C519

DATE	Rev	Description
0812	SA	Delete net SDVO_CTRL_DATA,SDVO_CTRL_CLK,R325,R326
0813	SA	J47 change from AO4422-1-GP(N-MOS) to P2003EVG-GP(P-MOS),delete Q31,R608,delete net VUSB_PU2 Add R628
0814	SA	Q29 OPEN for Intel recommend Q33 OPEN for Intel recommend Q8 OPEN
1002	1A	Change V_SM controller source to 5VDUAL (P.47) Correct on Board flash USB interface Add L7 to connect 1.2V power to E-SATA IC (P.37) Correct U8 to CN10 trace name for Marvell 88SE6111 Add R232 R255 Dummy resistor to disconnect HDD Power control by SIO Correct Front panel LAN LED control by LAN Active Pin (P.35) Add C9 to reserve HDD Power control sequency function (P.40) Correct LAN LED GIGA/100M connection Change RAID LED and Backup LED to GPIO 27, 28 Add EMI Cap (C12) for 1D8V_LAN power (P.35) Add EMI Cap (C10, C11) for CPU 12V power source (P.44) Add EMI Cap (C13) for CK_PE_100M_PCIE_SLOT (P.25)
	1B	Remove U47, C492, C491, R609, R607, C490 Q32 and connect V_5_USB to 5VDUAL to solve USB Vbus drop issue Re-layout CN22 Pin 13 and Pin 15 for connect 5VDUAL to Front Board change R391 to 820R to set current limit to 8A
	1B	Remove U6 R233 C214 to connect front LAN LED to LED_LAN_ACT directly no BOM change at -1A (20081023) For wake up issue, remove R521 and put R521 to R522 Add C14 and R233 for separate LAN connector GND from System GND
1014	1B	-1B Add net 1_KBDAT,1_KBCLK pull high 10K,for reserved @PAGE41
1212	1	Delete C14 and R233 for EMI Delete net 0 Add TC21 for reserved

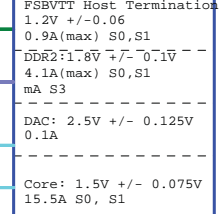
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Title REVISION HISTORY	
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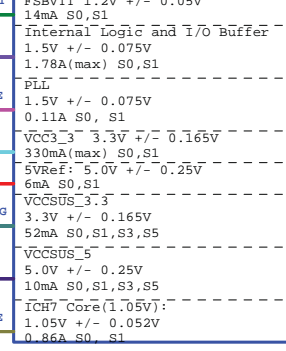
ATOM 230



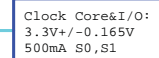
LAKE PORT 945GC



ICH7R



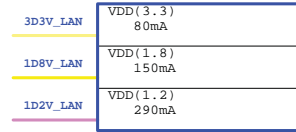
CK-410



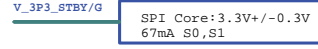
USB*4



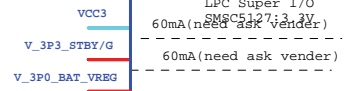
LAN 88E8071



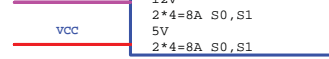
SPI



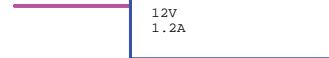
SIO



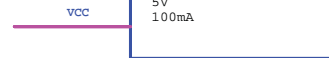
HDx4



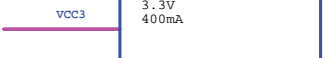
SYSTEM FAN



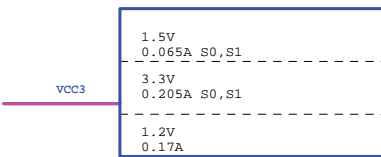
LED



SMI321



E-SATA



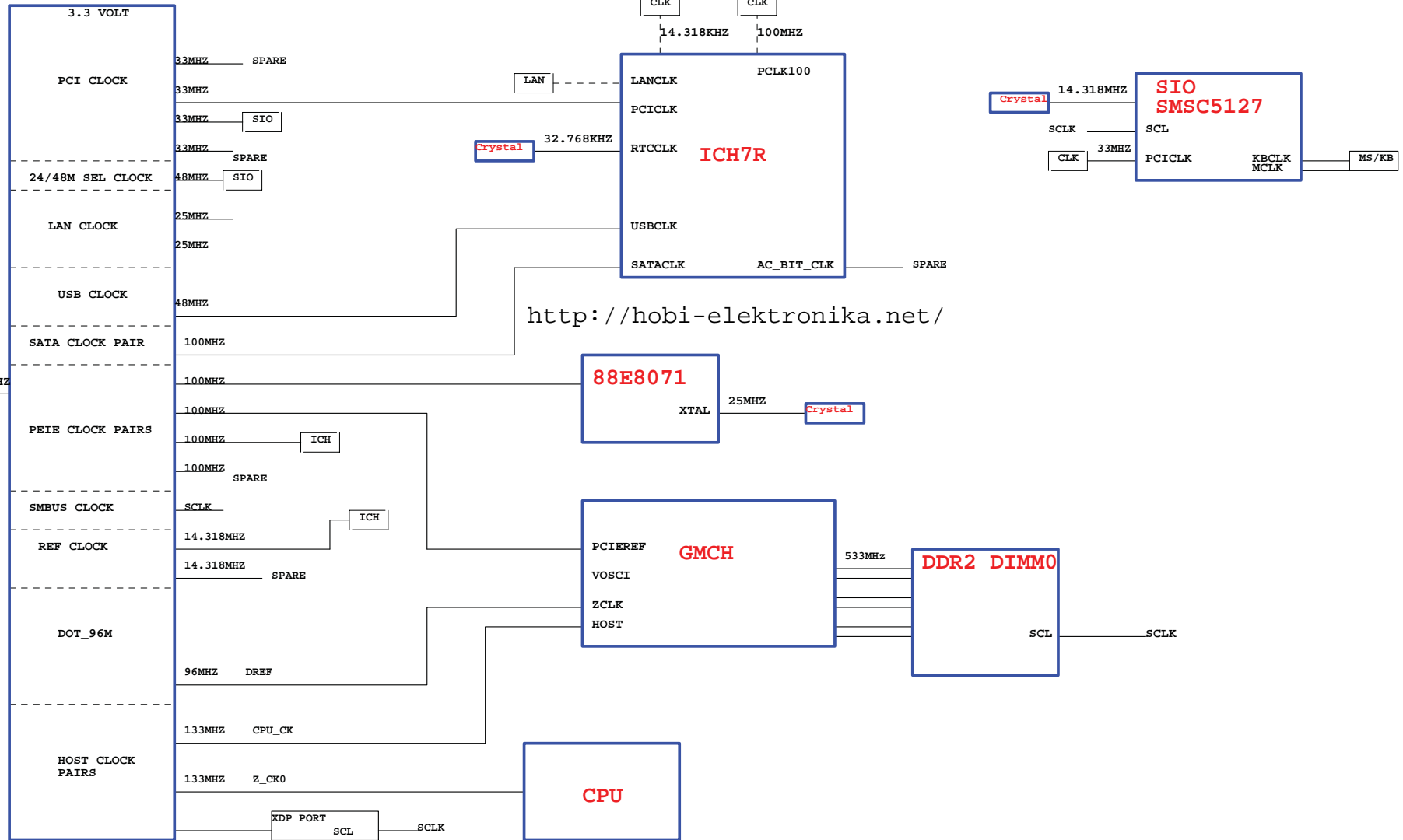
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wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd

File **POWER DISTRIBUTION** Hsichih, Taipei

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CK 410



疊構編號		4-1.6-7	注意事項	1. Impedance Control tolerance +/- 15%		
完成板厚 (mm)		1.6±0.16		2. Coupon 製作方式及 Impedance report 請依照Wistron規範製作		
Stack up				Impedance Request List		
<div><div>L1TOP</div><div>PP</div><div>L2GND/VCC</div><div>Core</div><div>L3GND/VCC</div><div>PP</div><div>L4Bottom</div></div>	<div><div>Thickness</div><div>(mil)</div><div>1.9</div><div>2.8</div><div>1.2</div><div>49.0</div><div>1.2</div><div>2.8</div><div>1.9</div></div>	Spec	Layer	L1	L4	
		Single Ended Type (Trace width : mil)				
			37.5Ω	7.5	7.5	
			40Ω	6.5	6.5	
			45Ω	5	5	
			50Ω	4	4	
		Remarks: 1. 成本考量.避免使用 線寬線距小於 4.9 mil以下設計.				
		2. "\ " 表示不建議在該層設計該特性阻抗值訊號線				
		Differential Type (Trace width/space/width: mil)				
			110Ω	\	\	
			100Ω	\	\	
			95Ω	3.9/8.1/3.9	3.9/8.1/3.9	
			90Ω	4.5/7.5/4.5=88.68	4.5/7.5/4.5=88.68	
			85Ω	\	\	
			80Ω	\	\	
	70Ω	\	\			
Total		60.8				

wistron

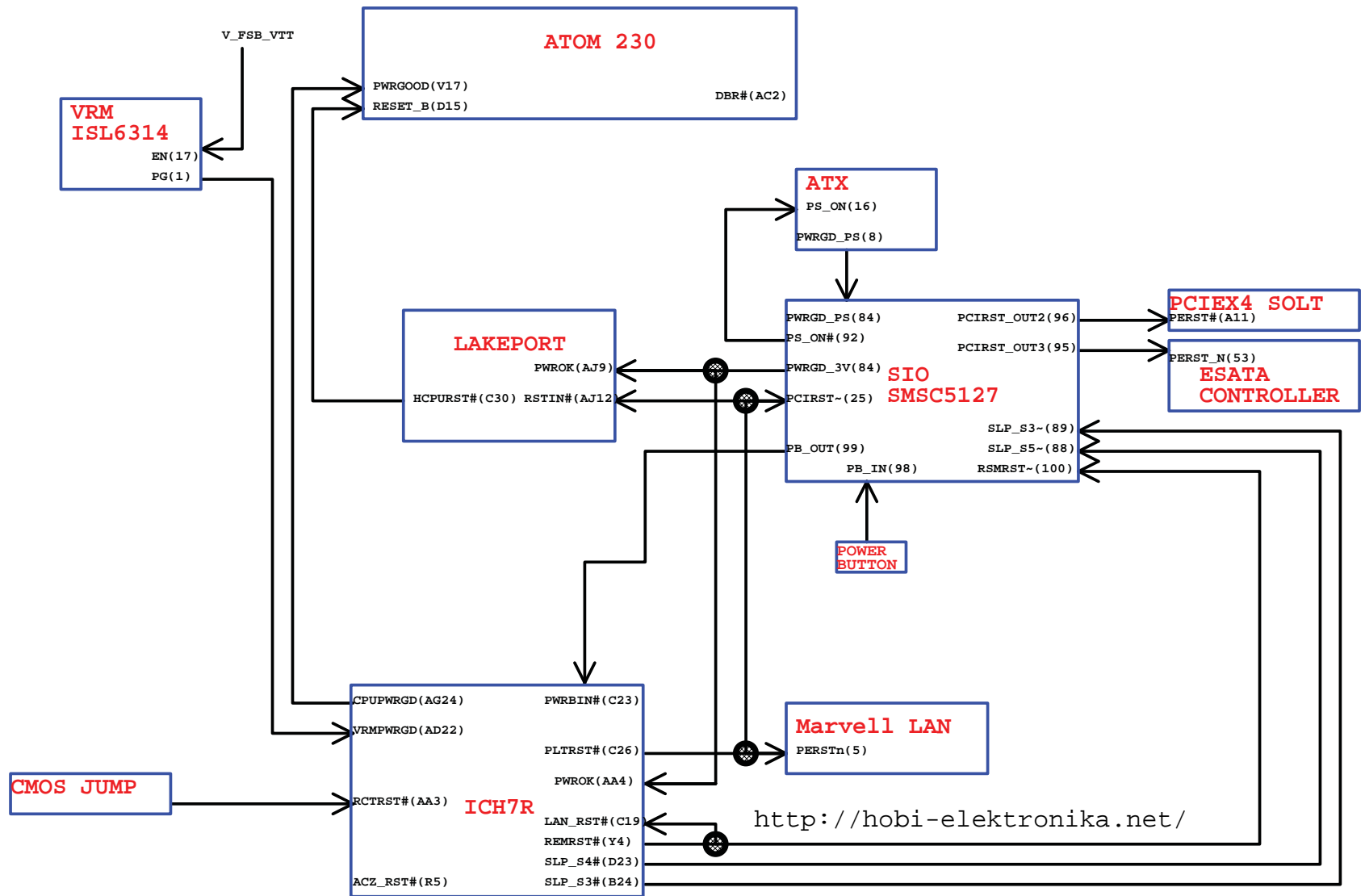
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Title Hsichih, Taipei

PCB STACK_UP

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RESET/POWER GOOD MAP

ICH 7R

PIN NAME	POWER WELL	USAGE	Default Type	DURING RESET	Enable Setting	DESCRIPTION	NOTES
GPIO0	MAIN	NO_USED	GPI	----	----		10K P/U TO VCC3 ON PAGE 28
GPIO1	MAIN	NO_USED	GPI	----	----		8.2K P/U TO VCC3 ON PAGE 34
GPIO2	MAIN	NO_USED	GPI	----	----		8.2K P/U TO VCC3 ON PAGE 34
GPIO3	MAIN	NO_USED	GPI	----	----		8.2K P/U TO VCC3 ON PAGE 34
GPIO4	MAIN	NO_USED	GPI	----	----		8.2K P/U TO VCC3 ON PAGE 34
GPIO5	MAIN	NO_USED	GPI	----	----		8.2K P/U TO VCC3 ON PAGE 34
GPIO6	MAIN	SMB321 Reset	GPI	----	----	Write protect for onboard flash	10K P/U TO VCC3 ON PAGE 31
GPIO7	MAIN	NO_USED	GPI	----	----		10K P/U TO VCC3 ON PAGE 31
GPIO8	RESUME	BACKUP_BUTTON	GPI	----	----	BACKUP DETECT	10K P/U TO V_3P3_STBYG ON PAGE 28
GPIO9	RESUME	2 PIN JUMPER	GPI	----	----	reserved function	10K P/U TO V_3P3_STBYG ON PAGE 28
GPIO10	RESUME	RESET_BUTTON	GPI	IN	----	RESET_BUTTON	10K P/U TO V_3P3_STBYG ON PAGE 28
GPIO11	RESUME	SMB_ALERT_PU	Native	----	----		10K P/U TO V_3P3_STBYG ON PAGE 31
GPIO12	RESUME	SIO_SMI_N	GPI	----	Low	System Management Interrupt from SIO	10K P/U TO V_3P3_STBYG ON PAGE 28
GPIO13	RESUME	PME_N	GPI	----	Low	PME from SIO	10K P/U TO V_3P3_STBYG ON PAGE 19
GPIO14	RESUME	NO_USED	GPI	IN	----		10K P/U TO V_3P3_STBYG ON PAGE 28
GPIO15	RESUME	MODEL_SELECT	GPI	----	Low	MODEL_SELECT JUMPER	
GPIO16	MAIN	NO_USED	GPO	----	----		----
GPIO17	MAIN	Root BIOS Destination Selection (SPI)	GPI	----	----	Root BIOS Destination Selection (SPI)	10K P/D TO GND ON PAGE 26
GPIO18	MAIN	NO_USED	GPO	----	----		connect to TP
GPIO19	MAIN	NO_USED	GPI	----	----		PULL UP 4K7 TO VCC3 ON PAGE27
GPIO20	MAIN	SYS_STATUS	GPO	----	Low	SYS_STATUS LED to Front Panel	
GPIO21	MAIN	NO_USED	GPI	----	----		PULL UP 4K7 TO VCC3 ON PAGE27
GPIO22	MAIN	NO_USED	Native	----	----		8.2K P/U TO VCC3 ON PAGE 34
GPIO23	MAIN	NO_USED	Native	----	----		connect to TP
GPIO24	RESUME	SYS_ERROR	GPO	----	Low	SYS_ERROR LED to Front Panel	
GPIO25	RESUME	PWR_LED	GPO	----	Low	PWR_LED to Front Panel	
GPIO26	RESUME	RAID_LED_CTRL	GPO	----	Low	RAID_LED_CTRL to Front Panel	
GPIO27	RESUME	BACKUP_STATUS	GPO	----	----		
GPIO28	RESUME	RAID_LED_CTRL2	GPO	----	----		
GPIO29	RESUME	USB OC5-	Native	----	----	Overcurrent Indicators	USB OC protect ON PAGE26
GPIO30	RESUME	USB OC6-	Native	----	----	Overcurrent Indicators (NO UESD)	8.2K P/U TO V_3P3_STBYG ON PAGE 26
GPIO31	RESUME	USB OC7-	Native	----	----	Overcurrent Indicators (NO UESD)	8.2K P/U TO V_3P3_STBYG ON PAGE 26
GPIO32	MAIN	NO_USED	GPO	----	----	BACKUP_STATUS LED	
GPIO33	MAIN	NO_USED	GPO	----	----	RAID_LED_CTRL2 to Front Panel	
GPIO34	MAIN	NO_USED	GPO	----	----		connect to TP
GPIO35	MAIN	NO_USED	GPO	----	----		connect to TP
GPIO36	MAIN	NO_USED	GPI	----	----		PULL UP 4K7 TO VCC3 ON PAGE27
GPIO37	MAIN	NO_USED	GPI	----	----		PULL UP 4K7 TO VCC3 ON PAGE27
GPIO38	MAIN	NO_USED	GPI	----	----		PULL UP 10K TO VCC3 ON PAGE28
GPIO39	MAIN	NO_USED	GPI	----	----		PULL UP 10K TO VCC3 ON PAGE28
GPIO40	NA	Not implemented.	NA	----	----		
GPIO41	NA	Not implemented.	NA	----	----		
GPIO42	NA	Not implemented.	NA	----	----		
GPIO43	NA	Not implemented.	NA	----	----		
GPIO44	NA	Not implemented.	NA	----	----		
GPIO45	NA	Not implemented.	NA	----	----		
GPIO46	NA	Not implemented.	NA	----	----		
GPIO47	NA	Not implemented.	NA	----	----		
GPIO48	MAIN	Root BIOS Destination Selection (SPI)	Native	----	----	Root BIOS Destination Selection (SPI)	10K P/U TO VCC3 ON PAGE 26
GPIO49	V_CPU_IO	H_PWRGD (Multi-function)	Native	----	----		

SMSC5127 I/O Address : 0x02E

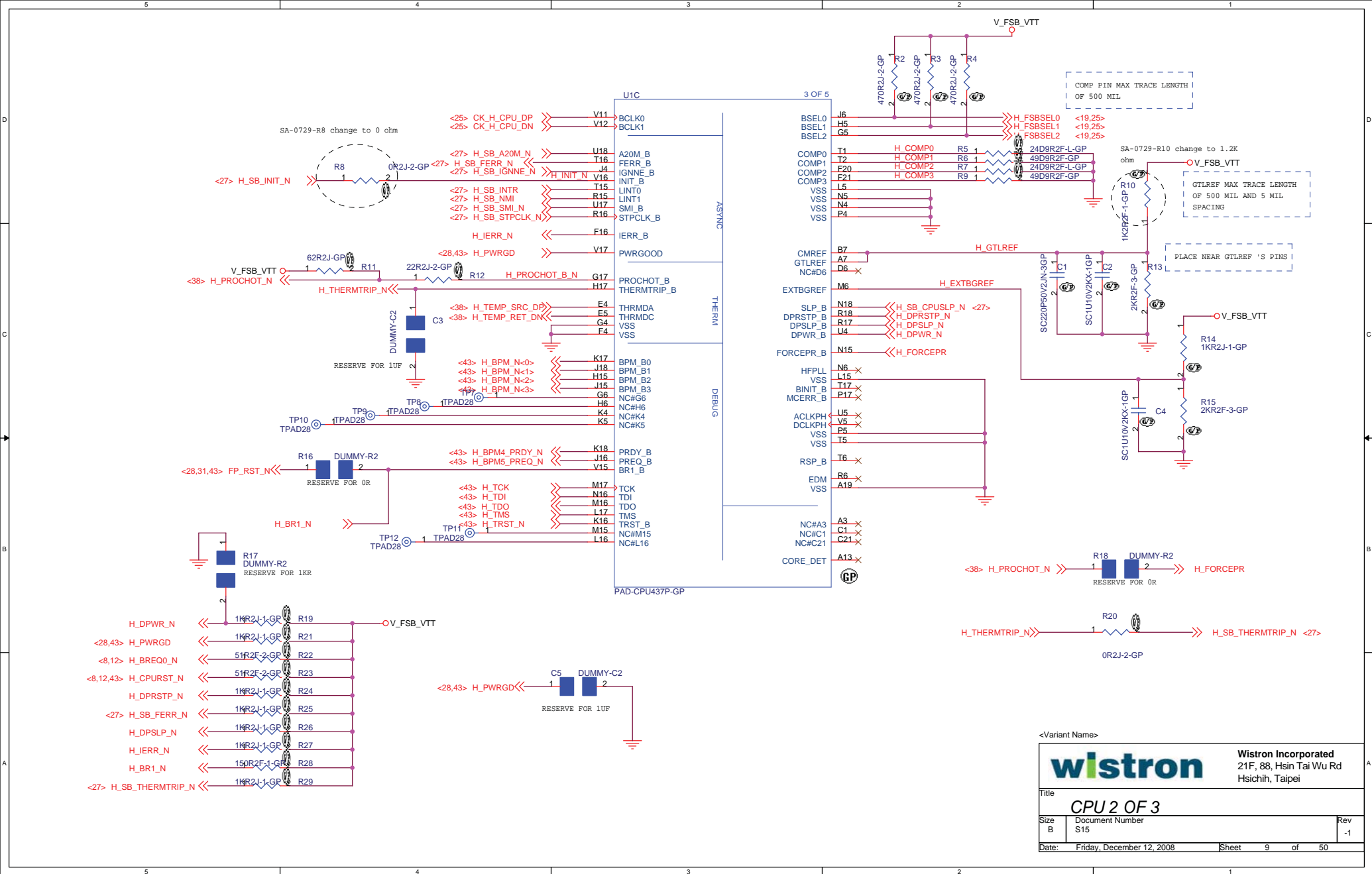
PIN NAME	POWER WELL	USAGE	DURING RESET	Enable Setting	DESCRIPTION	NOTES
GP10	MAIN	NO USED	OUT			CONNECT TO TP
GP11	RESUME	HDD4_BLUE		Low	HDD4 ACT	
GP12	RESUME	PLTRST_SLOTS_N	OUT	Low	PCIE SLOT RESET	10K P/U TO V_3P3_STBYG ON PAGE 38
GP13	RESUME	ESATA_RST_N	OUT		ESATA_RST_N	
GP14	RESUME	HDD4_AMBER	OUT		HDD4 FAIL	
GP15	MAIN	NO USED				
GP16	RESUME	SIO_PROCHOT_N	OUT	High	Control VR THERMAL THROTTLE CIRCUITRY ON PAGE28	PUSH PULL
GP17	RESUME	FAN_CTL3	OUT	Low	Control of POWER V_LED	----
GP20	MAIN	HWM_INT_N(reserve)	OUT	Low	Control Thermal Alarm in SB on Page19	10K PU on PAGE31
GP21	MAIN	SIO_KDAT	I/O	----	Keyboard Data I/O	
GP22	MAIN	SIO_KCLK	I/O	----	Keyboard Clock I/O	
GP27	MAIN	SIO_SMI_N	OUT	High		10K P/U TO 3P3_STBYG ON PAGE 38
GP32	MAIN	SIO_MDAT	I/O	----	Mouse Data I/O	
GP33	MAIN	SIO_MCLK	I/O	----	Mouse Clock I/O	
GP36	MAIN	KBRST_N	OUT	Low	Keyboard Reset Open-Drain Output	10K P/U TO VCC3 ON PAGE 38
GP37	MAIN	A20GATE	OUT	Low	Control A20GATE IN ICH9	10K P/U TO VCC3 ON PAGE 38
GP40	RESUME	PWRGD_ICH_SIO		Low	reserved function	Reserved 1K P/U TO VCC3 ON PAGE 28
GP41	RESUME	NO USED	OUT	----		
GP42	RESUME	SIO_PME_S3	OUT	High	Power Management Event Output.	10K P/U TO 3P3_STBYG ON PAGE 38
GP43	MAIN	NO USED	OUT	----	Front Panel Reset	10K P/U TO 3P3_STBYG ON PAGE 38
GP50	RESUME	HDD3_AMBER		----	HDD3 FAIL	
GP51	RESUME	HDD3_BLUE			HDD3 ACT	
GP52	RESUME	HDD2_AMBER		----	HDD2 FAIL	
GP53	RESUME	HDD2_BLUE	I/O	----	HDD2 ACT	
GP54	RESUME	NO USED	I/O	----		CONNECT TO TP
GP55	RESUME	NO USED	I/O			CONNECT TO TP
GP56	RESUME	HDD1_AMBER	I/O	----	HDD1 FAIL	
GP57	RESUME	HDD1_BLUE	I/O	----	HDD1 ACT	
GP60	RESUME	HDD3_PWR		----		330R P/U TO VCC ON PAGE 40
GP61	RESUME	HDD1_PWR		----		330R P/U TO V_3SB ON PAGE 40

GP10~GP17 are only an output and can not be configured as an input. GP60 and GP61 are OD output only.

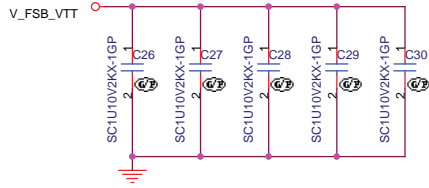
FLASH TYPE

GNT5#	GNT4#	Routing
0	1	Flash cycles routed to SPI
1	0	Flash cycles routed to PCI
1	1	Flash cycles routed to LPC

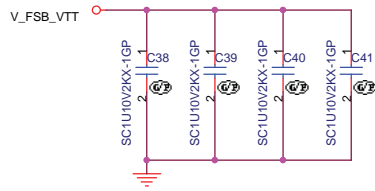
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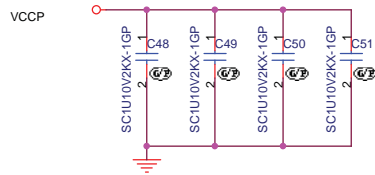
TOP SIDE CAPS FOR V_FSB_VTT PLANE



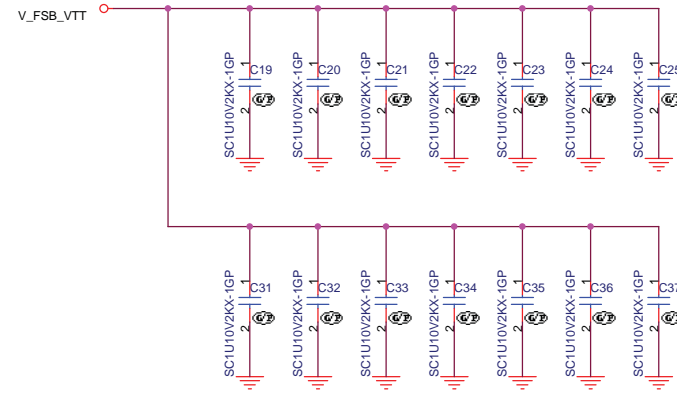
DECOUPLING FOR V_FSB_VTT



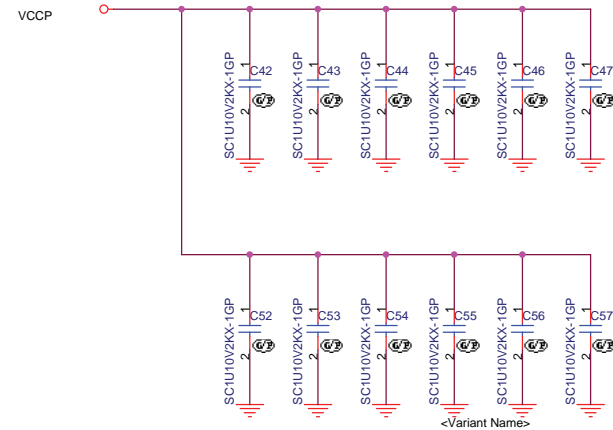
DECOUPLING FOR VCCP



BACKSIDE CAPS FOR V_FSB_VTT PLANE



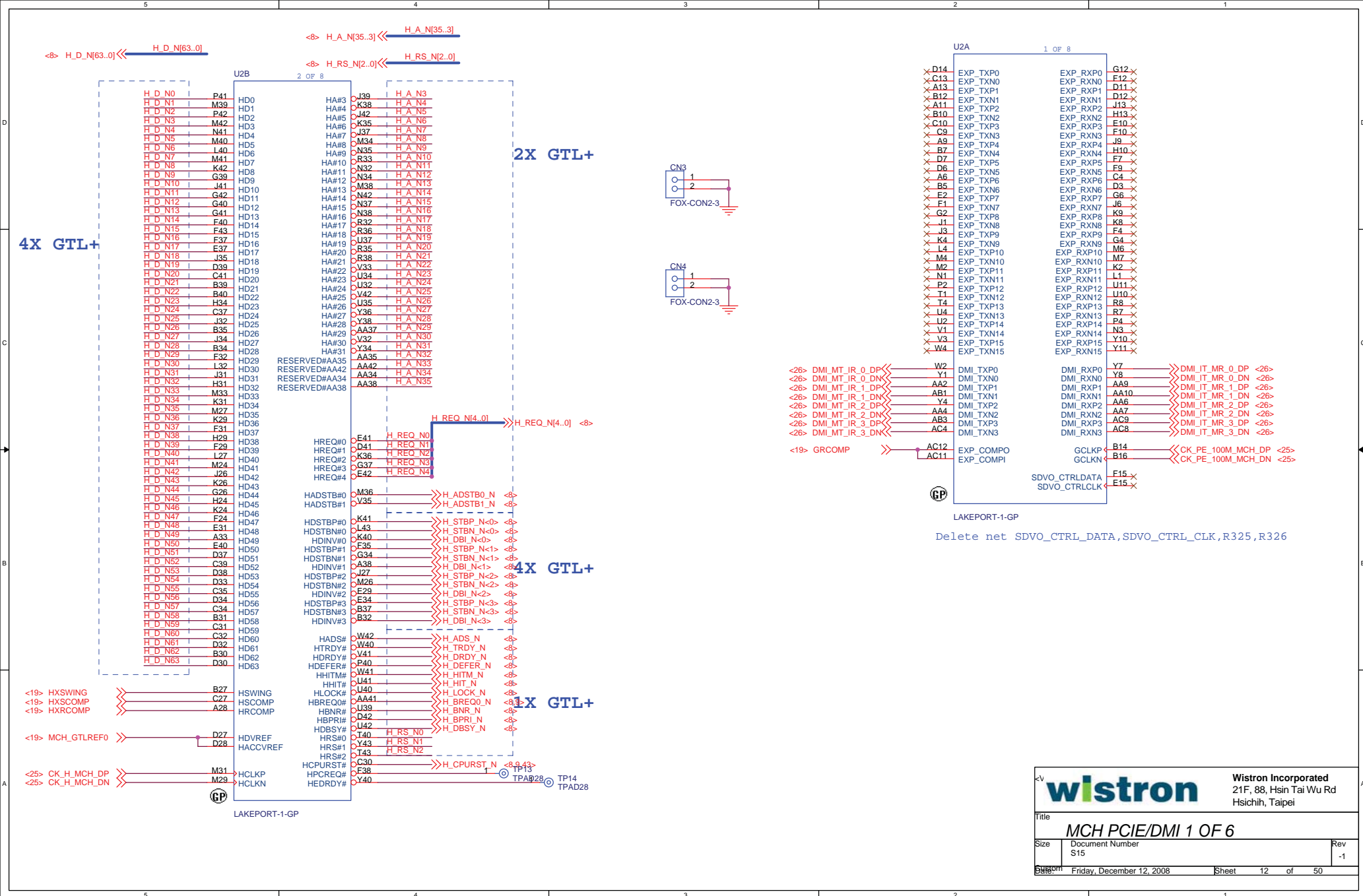
BACKSIDE CAPS FOR VCCP PLANE



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Title
CPU DECOUPLING CAPS

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<22.23> M_MAA_A[13..0] << M_MAA_A[13..0]

M_MAA_A0 BA32 SMA_A0
M_MAA_A1 AW32 SMA_A1
M_MAA_A2 BB30 SMA_A2
M_MAA_A3 BA30 SMA_A3
M_MAA_A4 AY30 SMA_A4
M_MAA_A5 BA27 SMA_A5
M_MAA_A6 BC26 SMA_A6
M_MAA_A7 AY27 SMA_A7
M_MAA_A8 AY26 SMA_A8
M_MAA_A9 BB27 SMA_A9
M_MAA_A10 AY33 SMA_A10
M_MAA_A11 AW27 SMA_A11
M_MAA_A12 BB26 SMA_A12
M_MAA_A13 BC38 SMA_A13

<22.23> M_WE_A_N << M_WE_A_N BB35 SWE_A#
<22.23> M_CAS_A_N << M_CAS_A_N BA32 SCAS_A#
<22.23> M_RAS_A_N << M_RAS_A_N BA34 SRA5_A#

<22.23> M_SBS_A0 << M_SBS_A0 RC33 SBS_A0
<22.23> M_SBS_A1 << M_SBS_A1 AY34 SBS_A1
<22.23> M_SBS_A2 << M_SBS_A2 BA26 SBS_A2

<22.23> M_SCS_A_NX << M_SCS_A_NX BB37 SCS_A#0
TP15 1 TPAD28 BA39 SCS_A#1
TP16 1 TPAD28 BA35 SCS_A#2
TP17 1 TPAD28 AY38 SCS_A#3

<22.23> M_SCKE_A0 << M_SCKE_A0 BB25 SCKE_A0
<22.23> M_SCKE_A1 << M_SCKE_A1 AY25 SCKE_A1
TP17 1 TPAD28 BC34 SCKE_A2
TP18 1 TPAD28 BA25 SCKE_A3

<22.23> M_ODT_A0 << M_ODT_A0 AW37 SODT_A0
<22.23> M_ODT_A1 << M_ODT_A1 AY39 SODT_A1
TP19 1 TPAD28 AY37 SODT_A2
TP20 1 TPAD28 BB40 SODT_A3

<22> CK_M_166M_DDR0_A_DP << BB32 SCLK_A0
<22> CK_M_166M_DDR0_A_DN << AY32 SCLK_A#0
<22> CK_M_166M_DDR1_A_DP << AY5 SCLK_A1
<22> CK_M_166M_DDR1_A_DN << BB5 SCLK_A#1
<22> CK_M_166M_DDR2_A_DP << AK42 SCLK_A2
<22> CK_M_166M_DDR2_A_DN << AK41 SCLK_A#2

TP21 1 TPAD28 BA31 SCLK_A3
TP20 1 TPAD28 BB31 SCLK_A#3
TP20 1 TPAD28 AY8 SCLK_A4
TP20 1 TPAD28 BA5 SCLK_A#4
TP20 1 TPAD28 AH40 SCLK_A5
TP20 1 TPAD28 AH43 SCLK_A#5

JBK16 RESERVED#BC16
XV14 RESERVED#W14
XW17 RESERVED#W17
XW18 RESERVED#W18

JBK40 RESERVED#AK40

<14.20> MCH_VREF_A >>> MCH_VREF_A AM4 SM_VREF_0

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TP28 1 TPAD28 AK17 RSV_TP0

SDQS_A0 AU14 M_DQS_A_DP0
SDQS_A#0 AR2 M_DQS_A_DN0
SDM_A0 AR3 M_DQM_A0

SDQ_A0 AP3 M_DATA_A0
SDQ_A1 AP2 M_DATA_A1
SDQ_A2 AU3 M_DATA_A2
SDQ_A3 AV4 M_DATA_A3
SDQ_A4 AN1 M_DATA_A5
SDQ_A5 AR4 M_DATA_A6
SDQ_A6 AU5 M_DATA_A6
SDQ_A7 AU2 M_DATA_A7

SDQS_A1 BA3 M_DQS_A_DP1
SDQS_A#1 BB4 M_DQS_A_DN1
SDM_A1 AY2 M_DQM_A1

SDQ_A8 AW3 M_DATA_A8
SDQ_A9 AY3 M_DATA_A9
SDQ_A10 BA7 M_DATA_A10
SDQ_A11 BB7 M_DATA_A11
SDQ_A12 AV1 M_DATA_A12
SDQ_A13 AW4 M_DATA_A13
SDQ_A14 BC5 M_DATA_A14
SDQ_A15 AY7 M_DATA_A15

SDQS_A2 AY11 M_DQS_A_DP2
SDQS_A#2 BA10 M_DQS_A_DN2
SDM_A2 BB10 M_DQM_A2

SDQ_A16 AW12 M_DATA_A16
SDQ_A17 AY10 M_DATA_A17
SDQ_A18 BA12 M_DATA_A18
SDQ_A19 BB12 M_DATA_A19
SDQ_A20 BA4 M_DATA_A20
SDQ_A21 BB8 M_DATA_A21
SDQ_A22 BC11 M_DATA_A22
SDQ_A23 AY12 M_DATA_A23

SDQS_A3 AU18 M_DQS_A_DP3
SDQS_A#3 AR18 M_DQS_A_DN3
SDM_A3 AP18 M_DQM_A3

SDQ_A24 AM20 M_DATA_A24
SDQ_A25 AM18 M_DATA_A25
SDQ_A26 AV20 M_DATA_A26
SDQ_A27 AM21 M_DATA_A27
SDQ_A28 AP17 M_DATA_A28
SDQ_A29 AR17 M_DATA_A29
SDQ_A30 AP20 M_DATA_A30
SDQ_A31 AT20 M_DATA_A31

SDQS_A4 AU35 M_DQS_A_DP4
SDQS_A#4 AV35 M_DQS_A_DN4
SDM_A4 AT34 M_DQM_A4

SDQ_A32 AP32 M_DATA_A32
SDQ_A33 AV34 M_DATA_A33
SDQ_A34 AV38 M_DATA_A34
SDQ_A35 AU39 M_DATA_A35
SDQ_A36 AV32 M_DATA_A36
SDQ_A37 AT32 M_DATA_A37
SDQ_A38 AR34 M_DATA_A38
SDQ_A39 AU37 M_DATA_A39

SDQS_A5 AP42 M_DQS_A_DP5
SDQS_A#5 AP40 M_DQS_A_DN5
SDM_A5 AP39 M_DQM_A5

SDQ_A40 AR41 M_DATA_A40
SDQ_A41 AR42 M_DATA_A41
SDQ_A42 AN43 M_DATA_A42
SDQ_A43 AM40 M_DATA_A43
SDQ_A44 AU41 M_DATA_A44
SDQ_A45 AU42 M_DATA_A45
SDQ_A46 AP41 M_DATA_A46
SDQ_A47 AN40 M_DATA_A47

SDQS_A6 AG42 M_DQS_A_DP6
SDQS_A#6 AG41 M_DQS_A_DN6
SDM_A6 AG40 M_DQM_A6

SDQ_A48 AL41 M_DATA_A48
SDQ_A49 AL42 M_DATA_A49
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SDQ_A51 AE40 M_DATA_A51
SDQ_A52 AM41 M_DATA_A52
SDQ_A53 AM42 M_DATA_A53
SDQ_A54 AE41 M_DATA_A54
SDQ_A55 AE42 M_DATA_A55

SDQS_A7 AC42 M_DQS_A_DP7
SDQS_A#7 AC41 M_DQS_A_DN7
SDM_A7 AC40 M_DQM_A7

SDQ_A56 AD40 M_DATA_A56
SDQ_A57 AD43 M_DATA_A57
SDQ_A58 AA39 M_DATA_A58
SDQ_A59 AA40 M_DATA_A59
SDQ_A60 AE42 M_DATA_A60
SDQ_A61 AE41 M_DATA_A61
SDQ_A62 AB41 M_DATA_A62
SDQ_A63 AB42 M_DATA_A63

LAKEPORT-1-GP



U2D 4 OF 8		
BB22	SMA_B0	SDQS_B0 AM8
BB21	SMA_B1	SDQS_B#0 AM8
BA21	SMA_B2	SDM_B0 AL1
AV21	SMA_B3	
AC20	SMA_B5	SDQ_B0 AL6
AY19	SMA_B4	SDQ_B1 AL8
BA18	SMA_B6	SDQ_B2 AP8
BA19	SMA_B7	SDQ_B3 AP9
BB18	SMA_B8	SDQ_B4 AL11
BA22	SMA_B9	SDQ_B5 AL9
BB17	SMA_B10	SDQ_B6 AM10
BA17	SMA_B11	SDQ_B7 AP8
AV42	SMA_B12	
BA13	SMA_B13	SDQS_B1 AV7
BB23	SWE_B#	SDQS_B#1 AS8
AY24	SCAS_B#	SDM_B1 AW2
BA23	SRAS_B#	
AV23	SBS_B0	SDQ_B8 AU7
AY23	SBS_B1	SDQ_B9 AV6
AV17	SBS_B2	SDQ_B10 AV14
BA40		SDQ_B11 AM1
AV41	SCS_B0#	SDQ_B12 AS5
BA41	SCS_B1#	SDQ_B13 AR7
AV40	SCS_B2#	SDQ_B14 AR14
BA40	SCS_B3#	SDQ_B15 AR10
BA14	SCKE_B0	SDQS_B2 AV13
AV16	SCKE_B1	SDQS_B#2 AT13
BA13	SCKE_B2	SDM_B2 AP13
BB13	SCKE_B3	
AV42	SODT_B0	SDQ_B16 AM15
AV40	SODT_B1	SDQ_B17 AM1
AV43	SODT_B2	SDQ_B18 AV15
AV40	SODT_B3	SDQ_B19 AM12
		SDQ_B20 AM1
		SDQ_B21 AR13
		SDQ_B22 AP15
		SDQ_B23 AT1
		SDQS_B3 AU23
		SDQS_B#3 AR23
		SDM_B3 AP23
		SDQ_B24 AM24
		SDQ_B25 AM23
		SDQ_B26 AV24
		SDQ_B27 AM26
AM23	SCLK_B0	SDQ_B28 AP2
AV27	SCLK_B#0	SDQ_B29 AP2
AV9	SCLK_B#1	SDQ_B30 AP24
AL38	SCLK_B2	SDQ_B31 AT23
AL36	SCLK_B3	
AP26	SCLK_B#2	SDQS_B4 AT23
AV26	SCLK_B#3	SDQS_B#4 AV23
AU10	SCLK_B4	SDM_B4 AR24
AT10	SCLK_B#4	
AL38	SCLK_B5	SDQ_B32 AU27
AL36	SCLK_B#5	SDQ_B33 AN28
		SDQ_B34 AR1
		SDQ_B35 AM11
		SDQ_B36 AP27
		SDQ_B37 AR27
		SDQ_B38 AP13
		SDQ_B39 AU3
		SDQS_B5 AP36
		SDQS_B#5 AM36
AL39	RESERVED#AL39	SDM_B5 AR36
		SDQ_B40 AP35
		SDQ_B41 AP37
		SDQ_B42 AN34
		SDQ_B43 AL35
		SDQ_B44 AR35
		SDQ_B45 AU38
		SDQ_B46 AM38
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		SDQ_B49 AL34
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		SDQ_B52 AL31
		SDQ_B53 AL36
		SDQ_B54 AG36
		SDQ_B55 AD36
AK19	RSV_TP3	
AK23	RSV_TP2	
		SDQS_B7 AD36
		SDQS_B#7 AD36
		SDM_B7 AD36
		SDQ_B56 AC32
		SDQ_B57 AD34
		SDQ_B58 AC3
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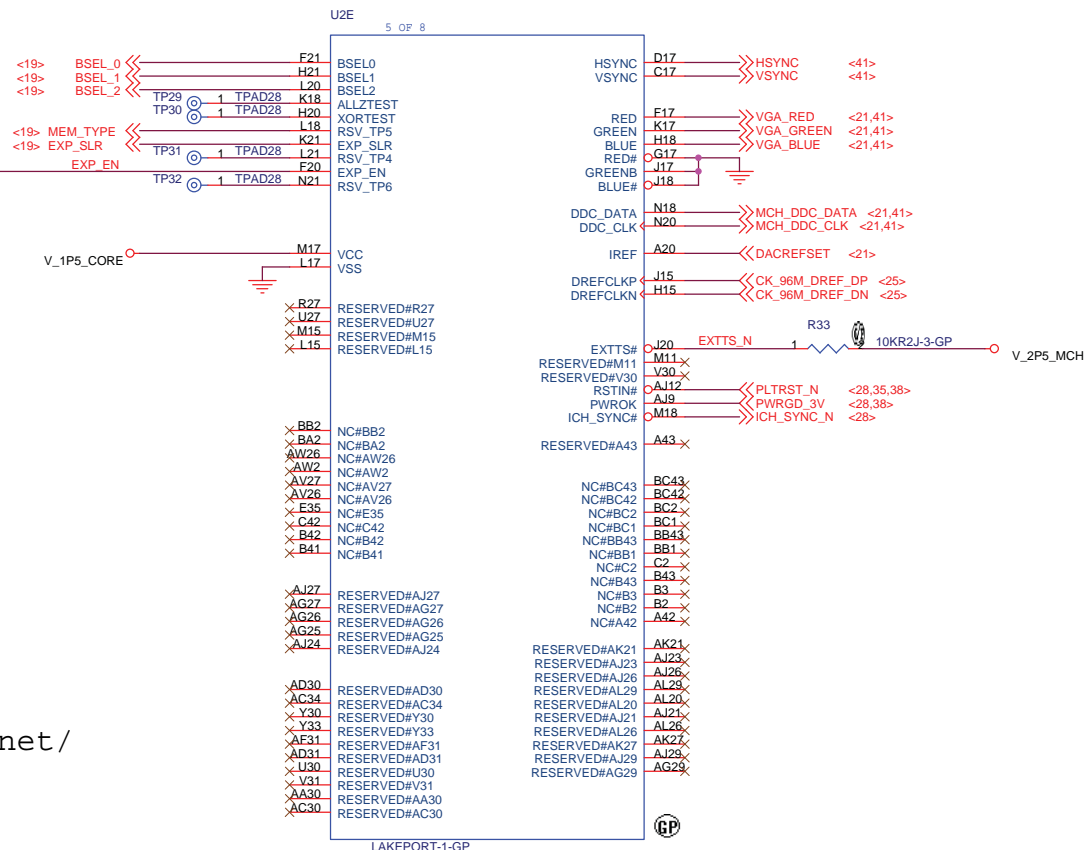
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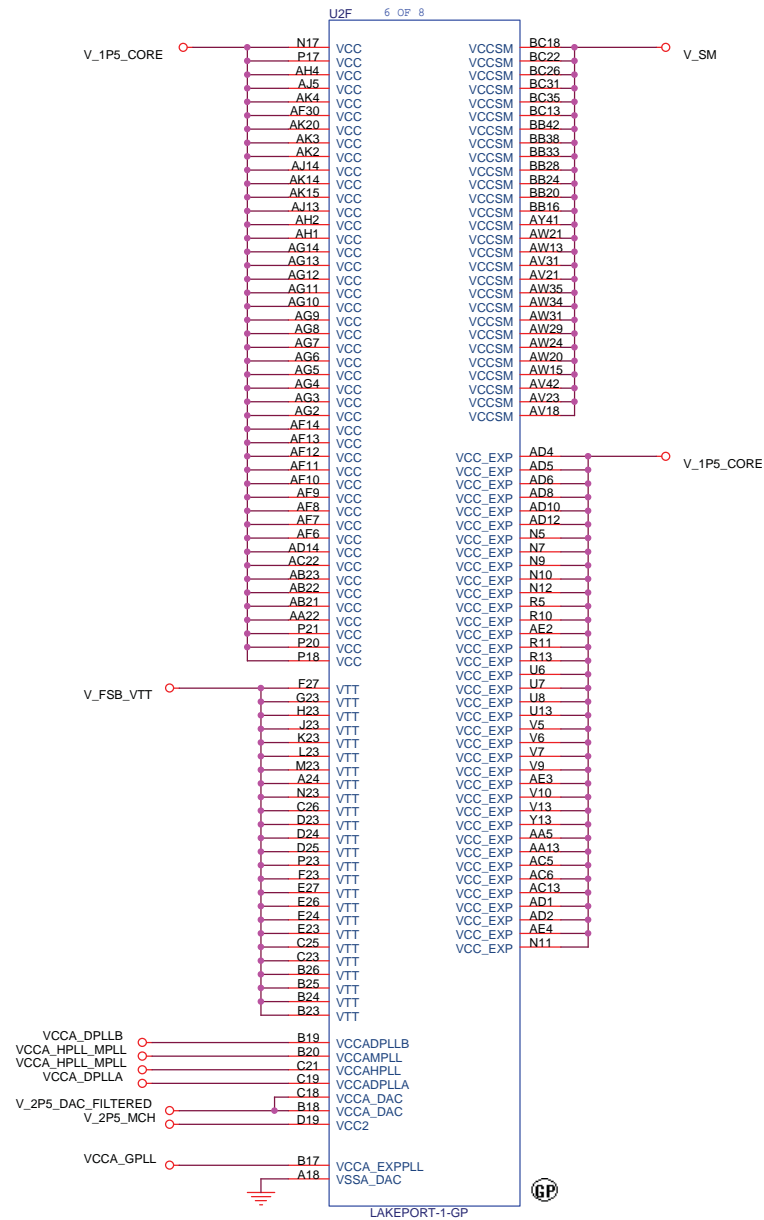
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 <20> SMRCOMP_N >> AL6 SM_OCDCOMP_0
 >> AL5 SM_RCOMP0

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SIGNAL NAMING CONVENTION

EXP : PCI EXPRESS
 DMI : DIRECT MEDIA INTERFACE
 ITP : ICH TRANSMIT POSITIVE
 ITN : ICH TRANSMIT NEGATIVE
 IRP : ICH RECEIVE POSITIVE
 IRN : ICH RECEIVE NEGATIVE
 MTP : MCH TRANSMIT POSITIVE
 MTN : MCH TRANSMIT NEGATIVE
 MRP : MCH RECEIVE POSITIVE
 MRN : MCH RECEIVE NEGATIVE



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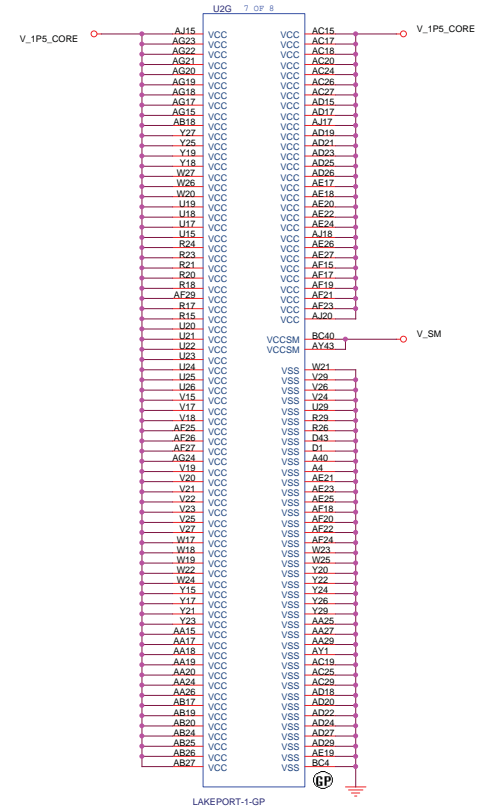
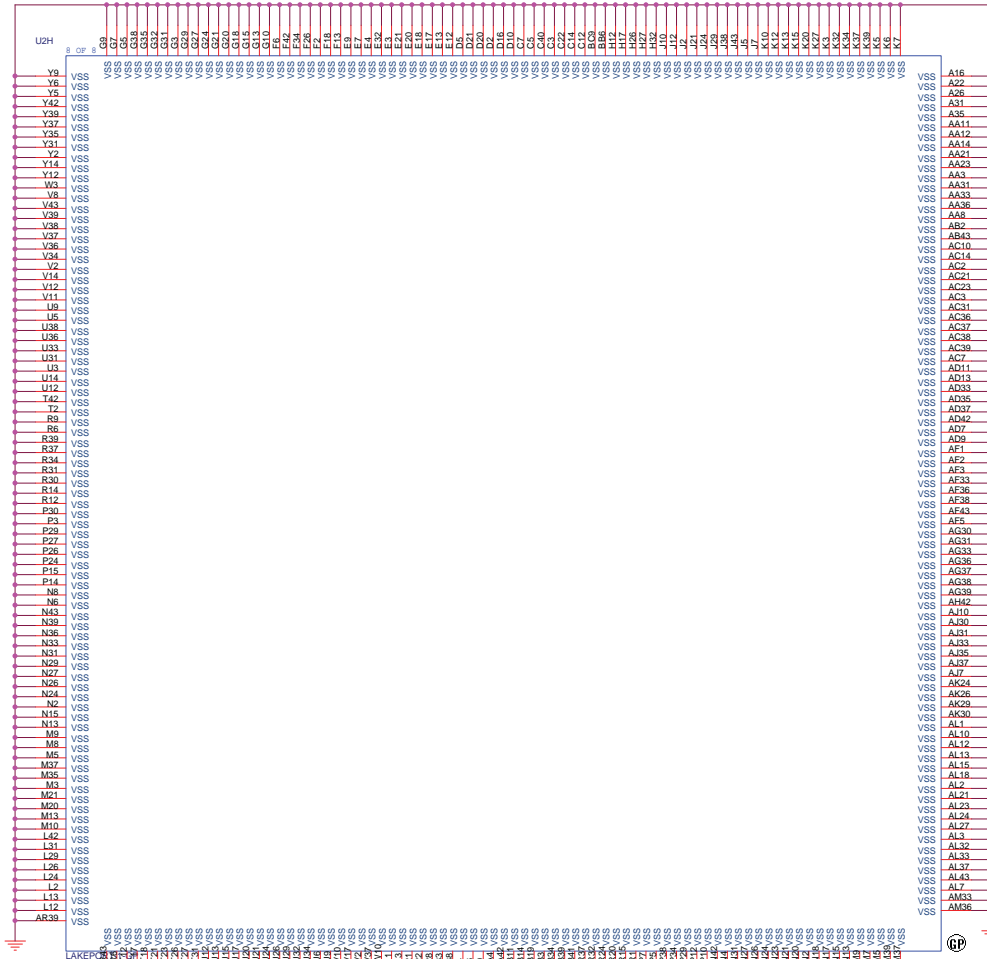
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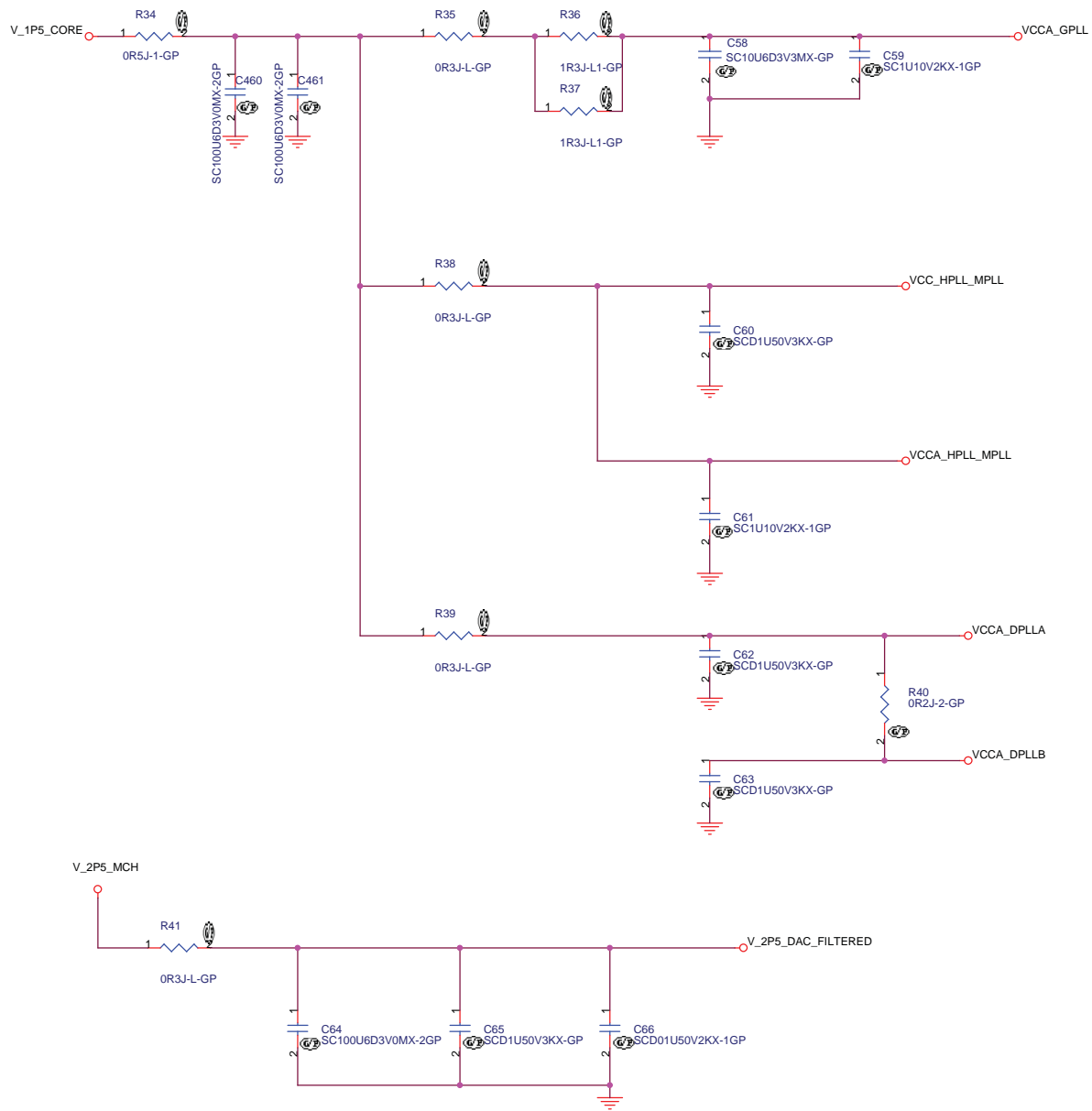
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MCH 2P5_DAC & PLL FIL TERS

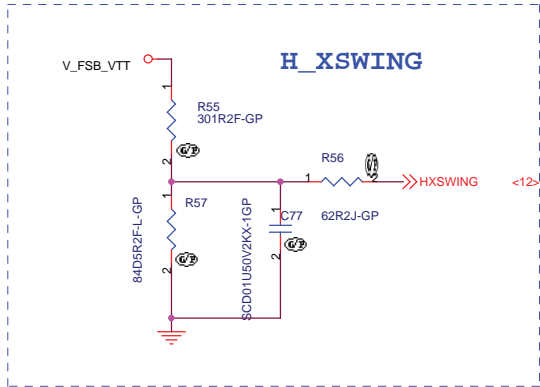
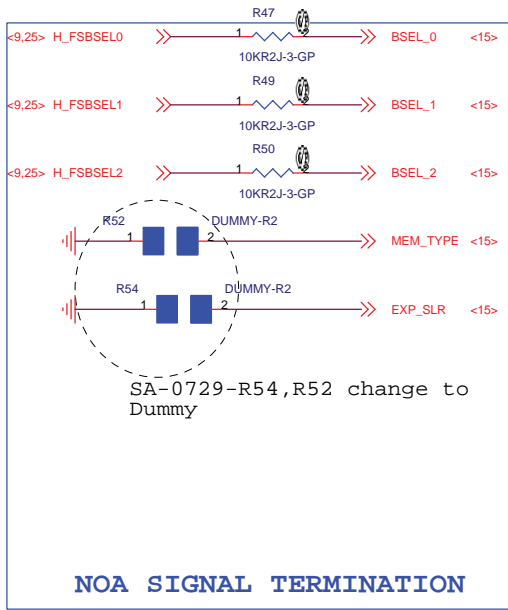
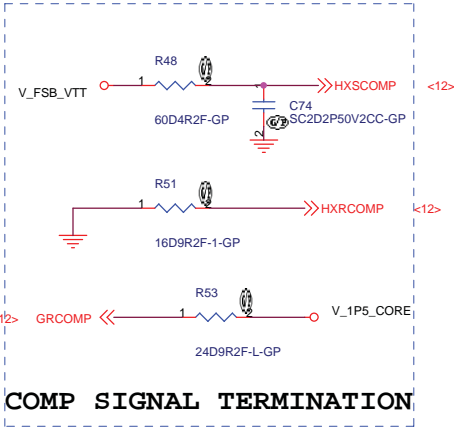
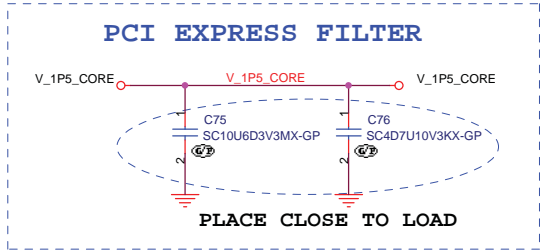
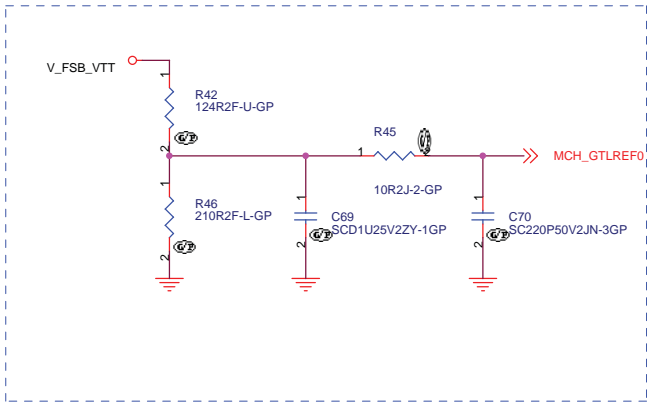
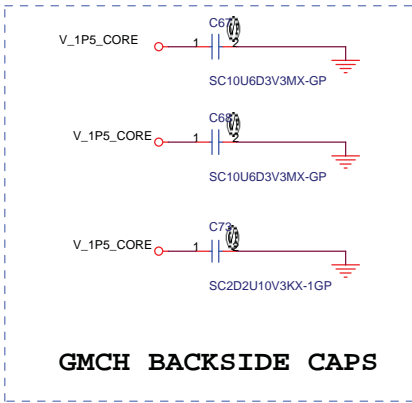
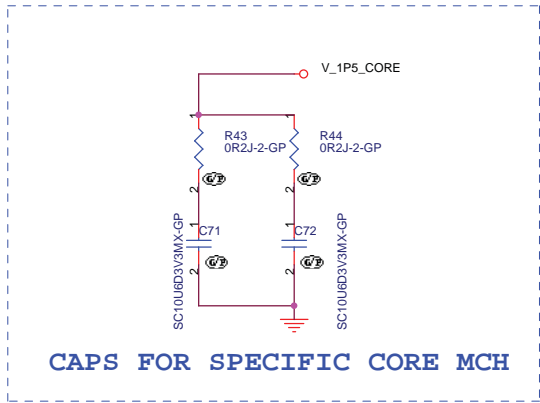
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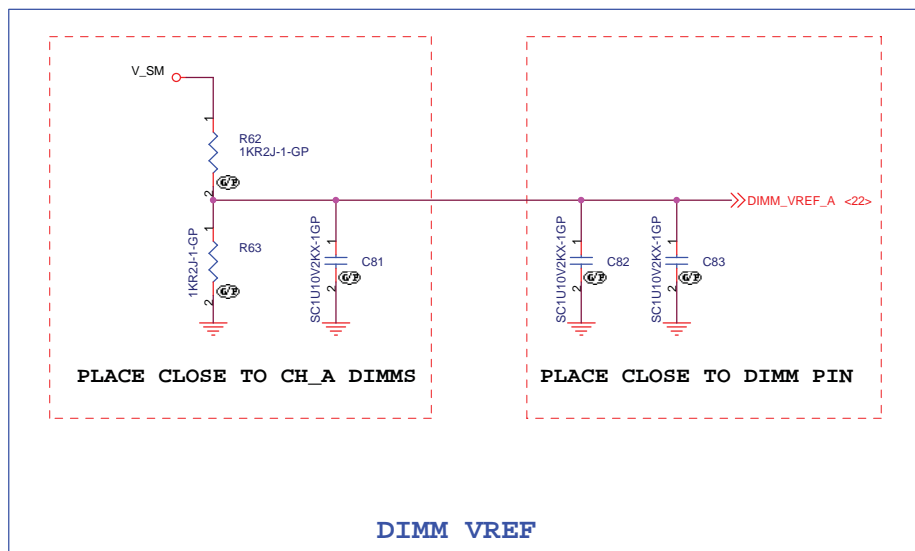
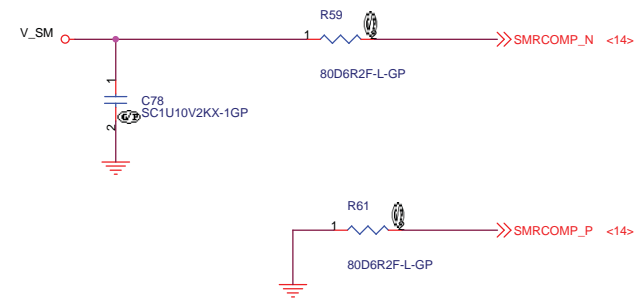
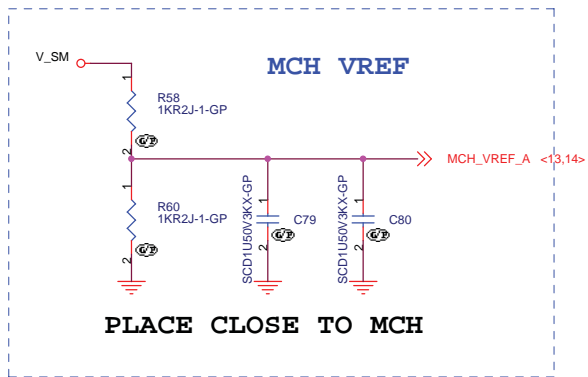
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MCH & DIMM VREF & COMP

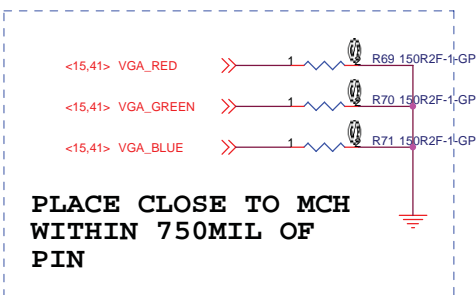
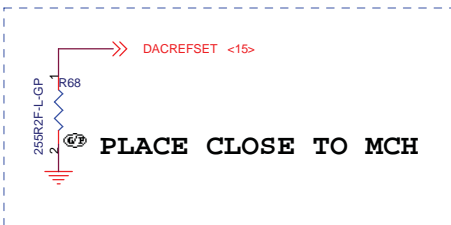
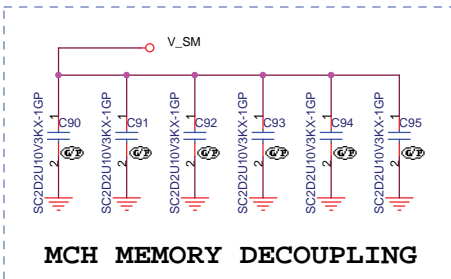
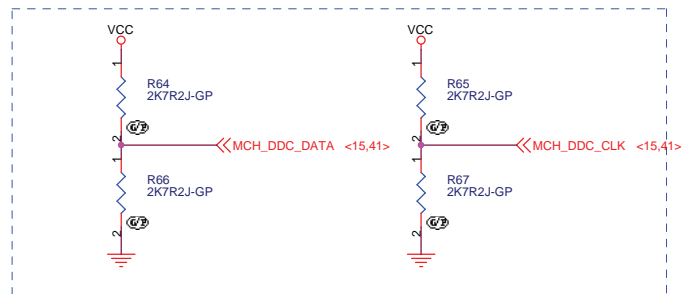
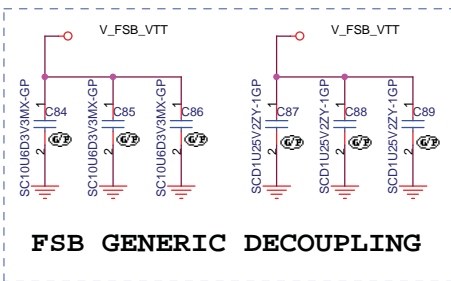
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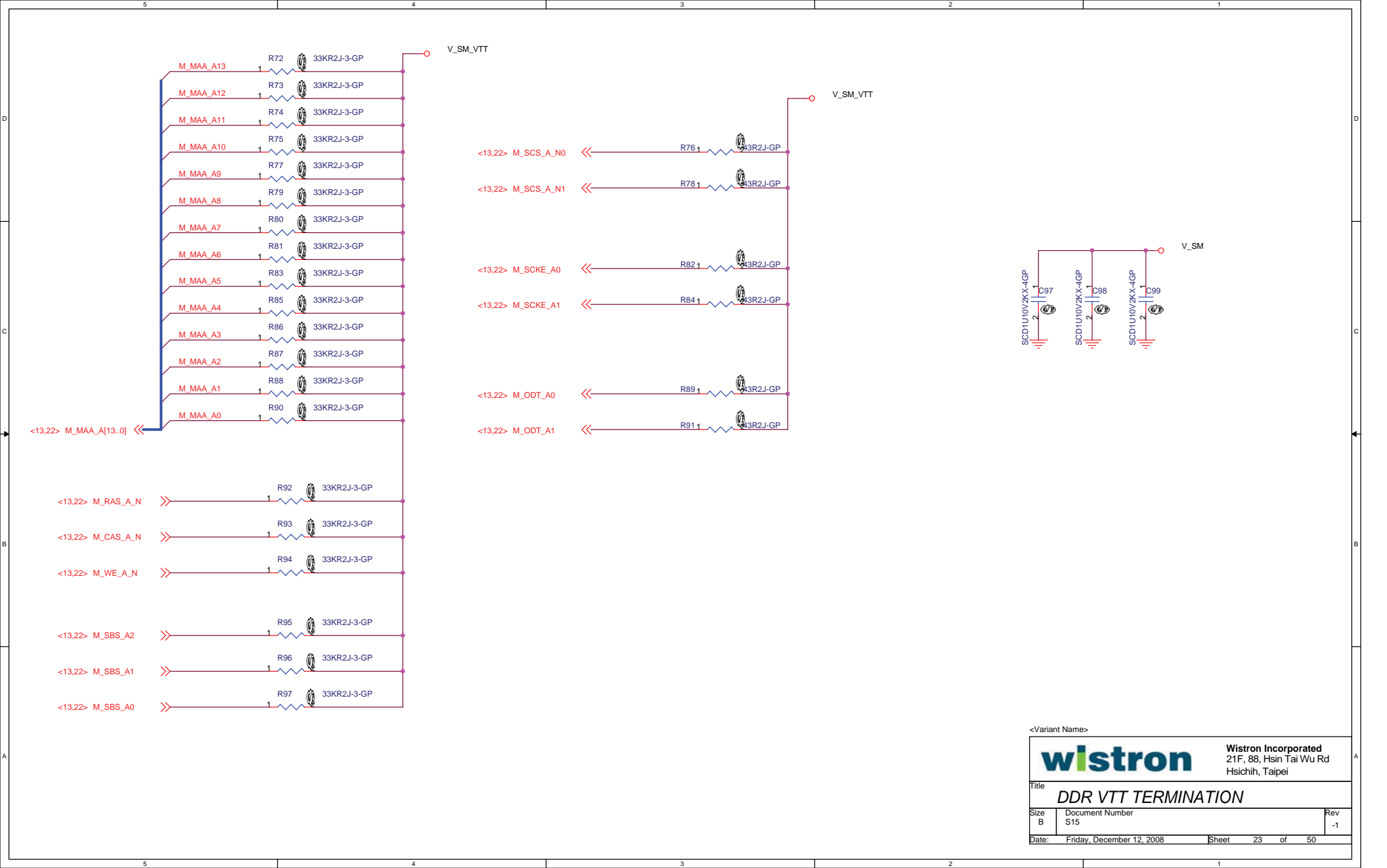
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**VGA TRACE DEFINITION SHOULD
BE THE SAME WITH SJ-D4**

SA-0730-change R69,R70,R71 to 150 Ohm

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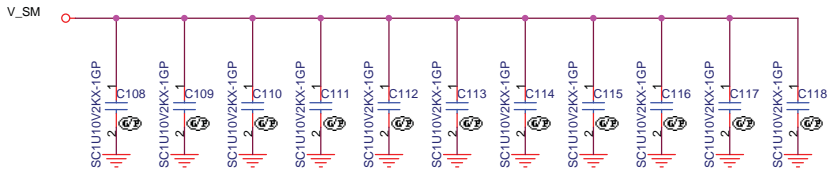
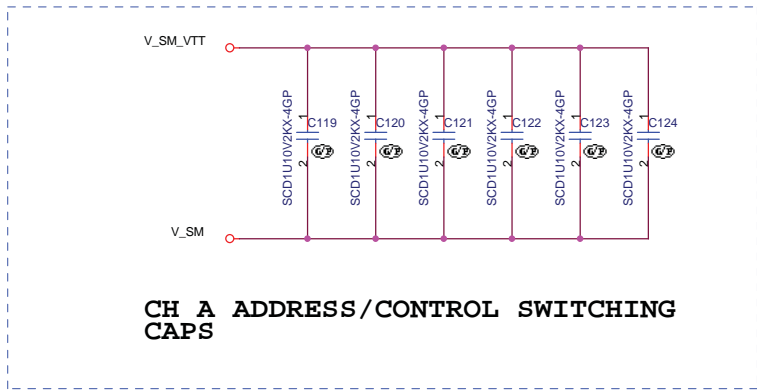
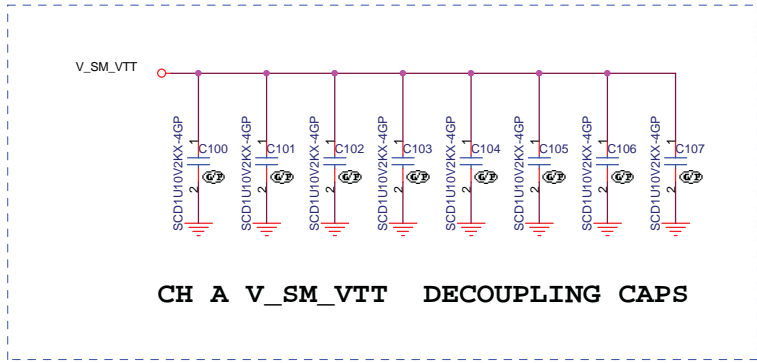
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DDR VTT DECOUPLING

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SA-0730-delete Net CK410_VDDPCI, and change to VDD_SRC_CLKA

PLACE PER PIN

VDD_SRC_CLKA

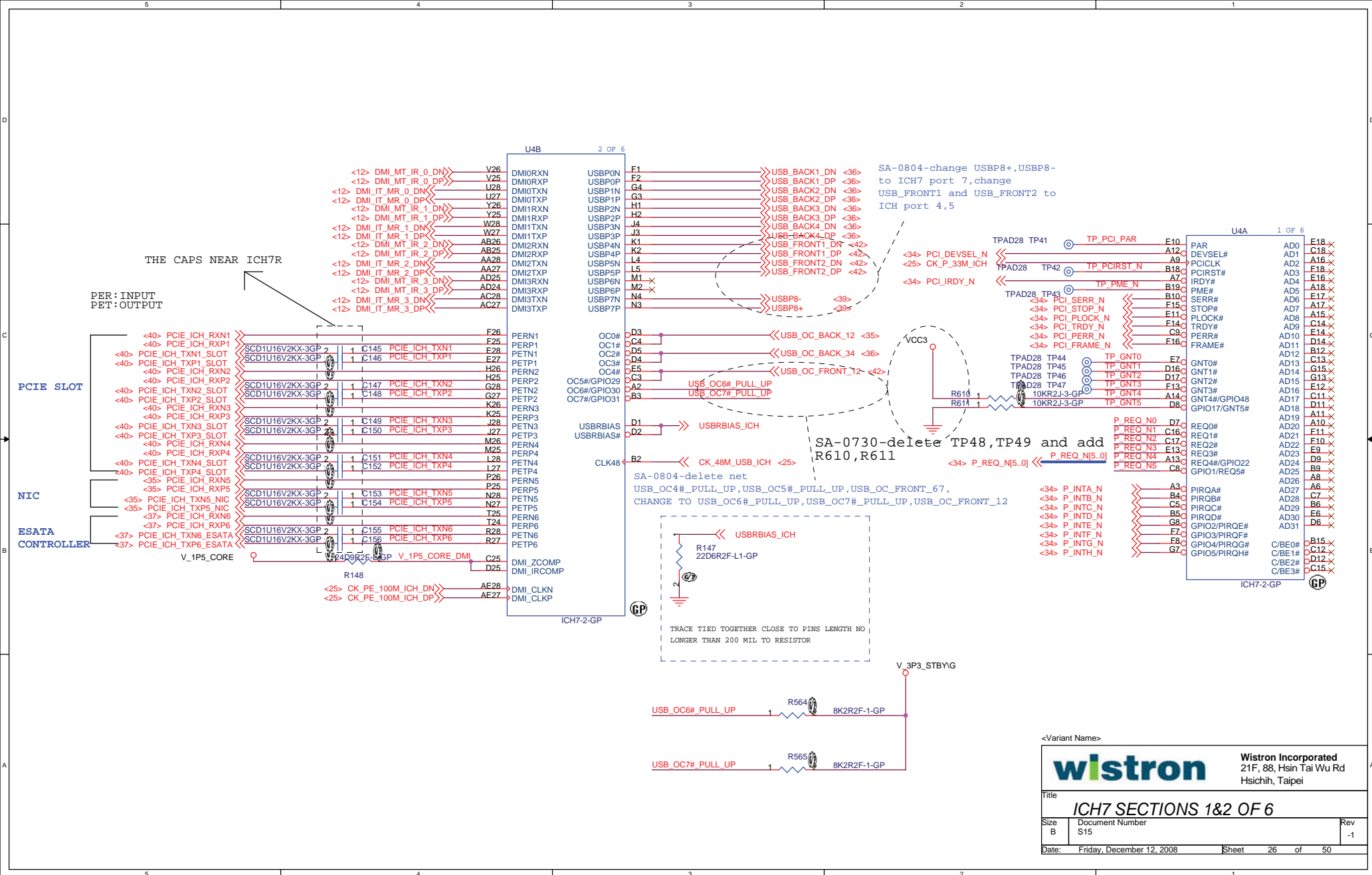
SA-0730-change R129 to 33 ohm

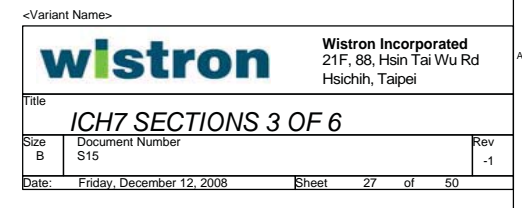
SA-0730-change R146 to DUMMY

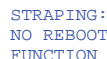
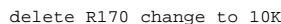
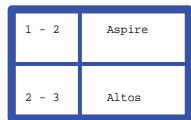
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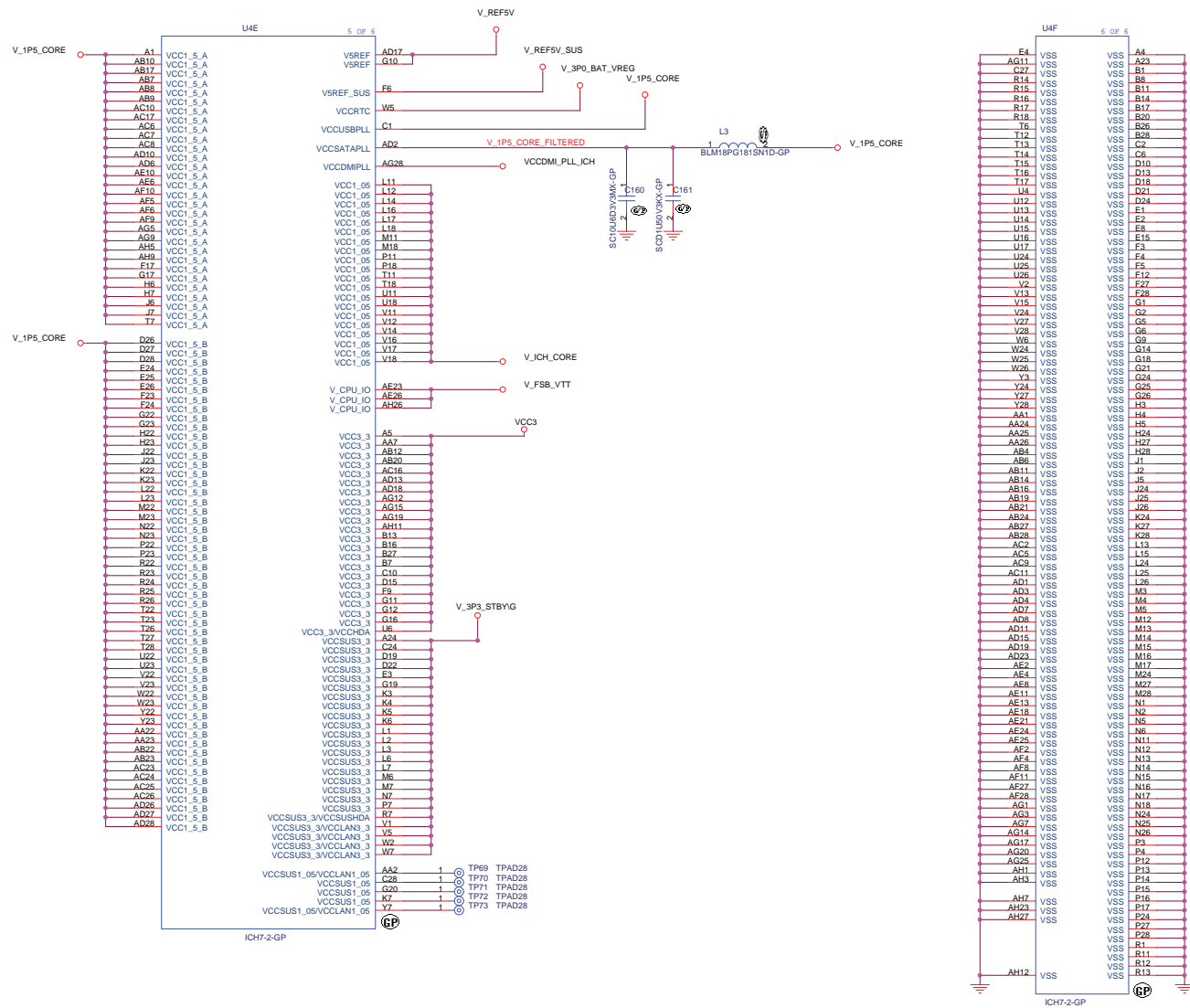
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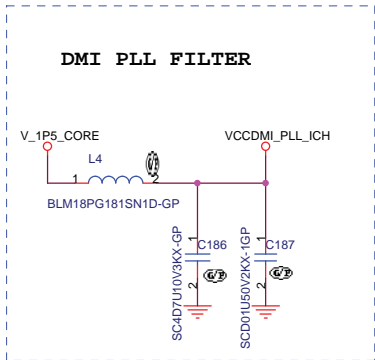
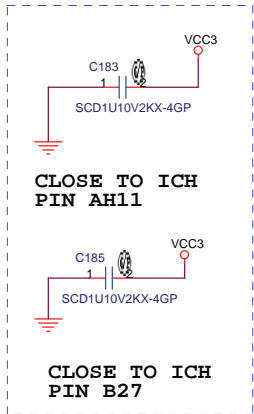
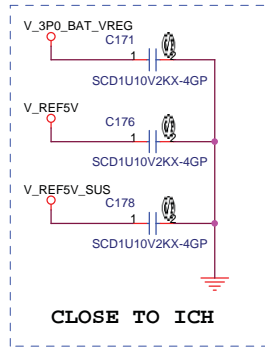
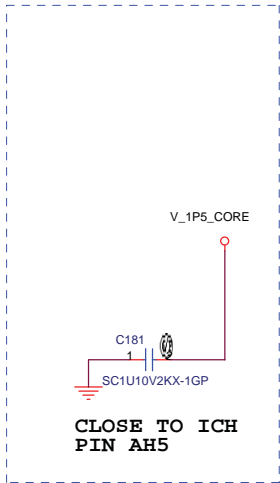
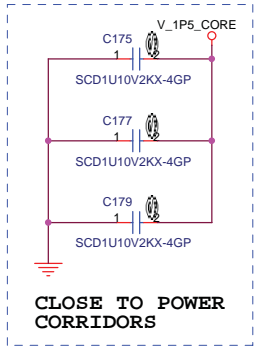
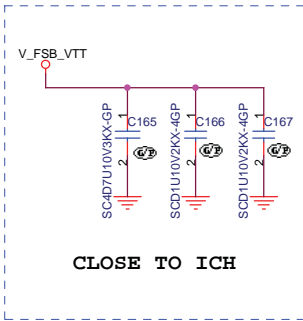
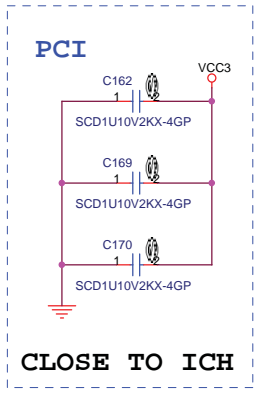


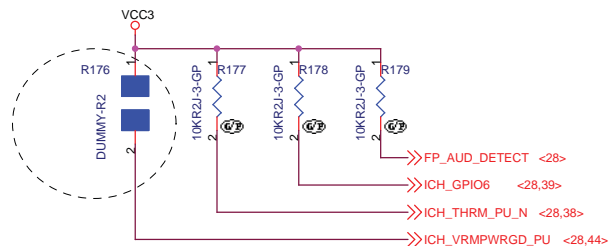
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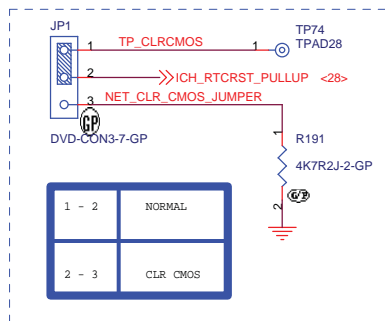
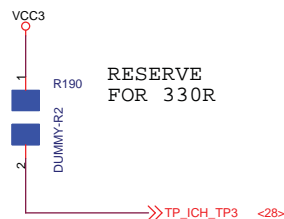
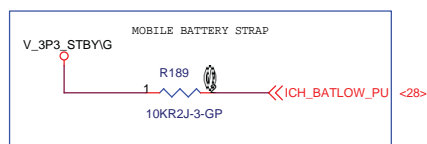
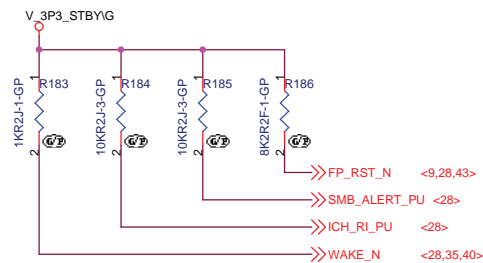
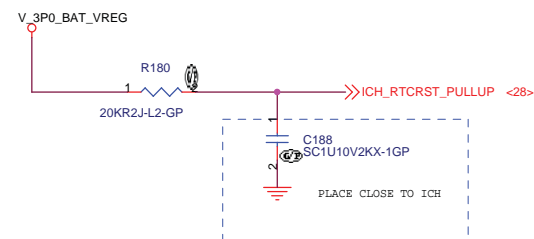
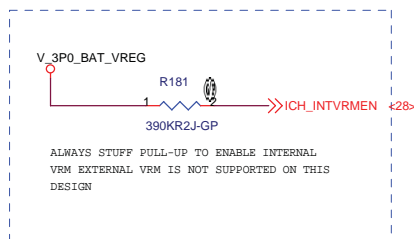
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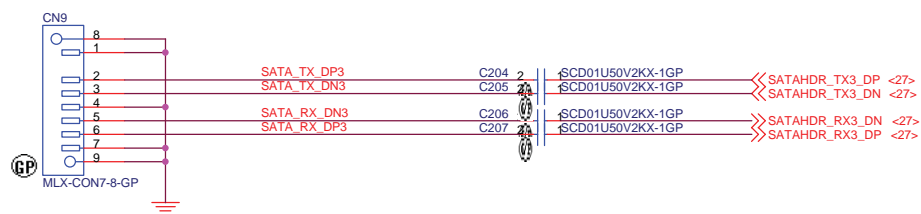
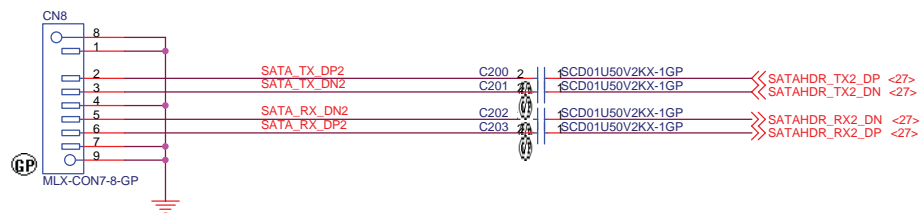
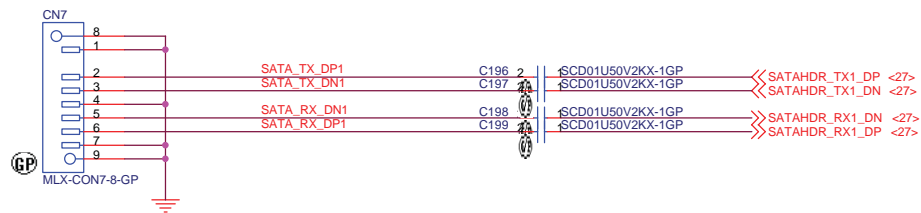
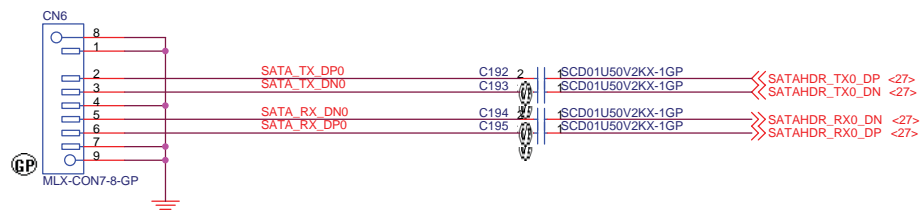
R176 change to Dummy, for VRM's power good already pull high



<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title ICH PULL UP		
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<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

SATA CONNECTOR

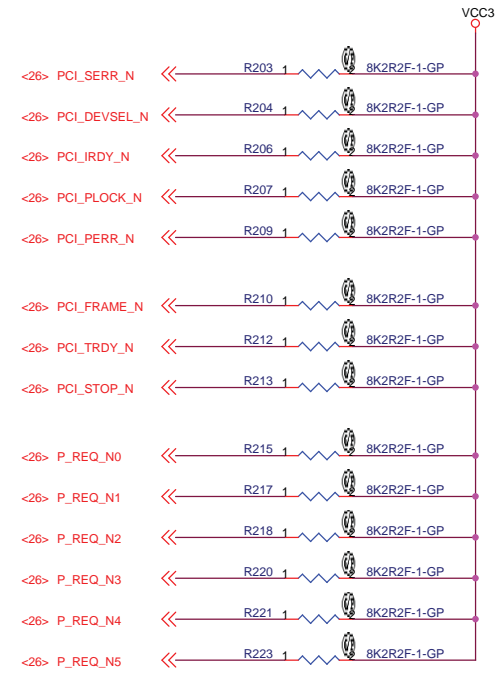
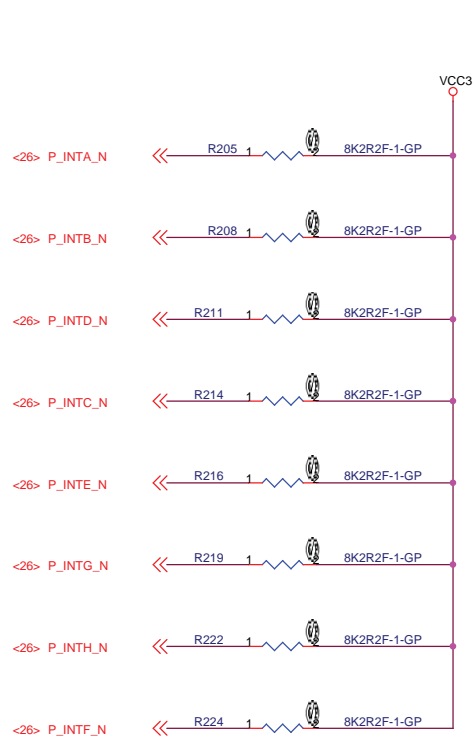
Size
B

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-1

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<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

PCI TERMINATION

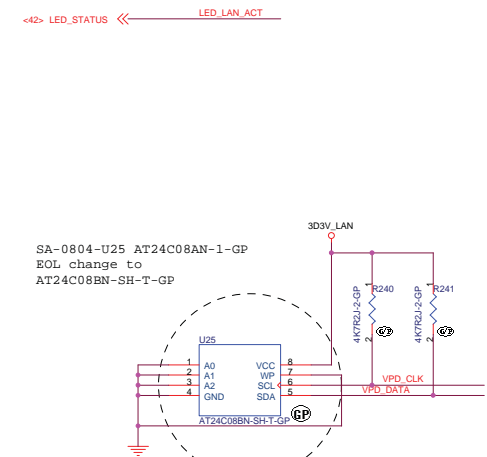
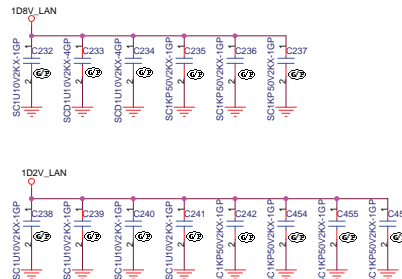
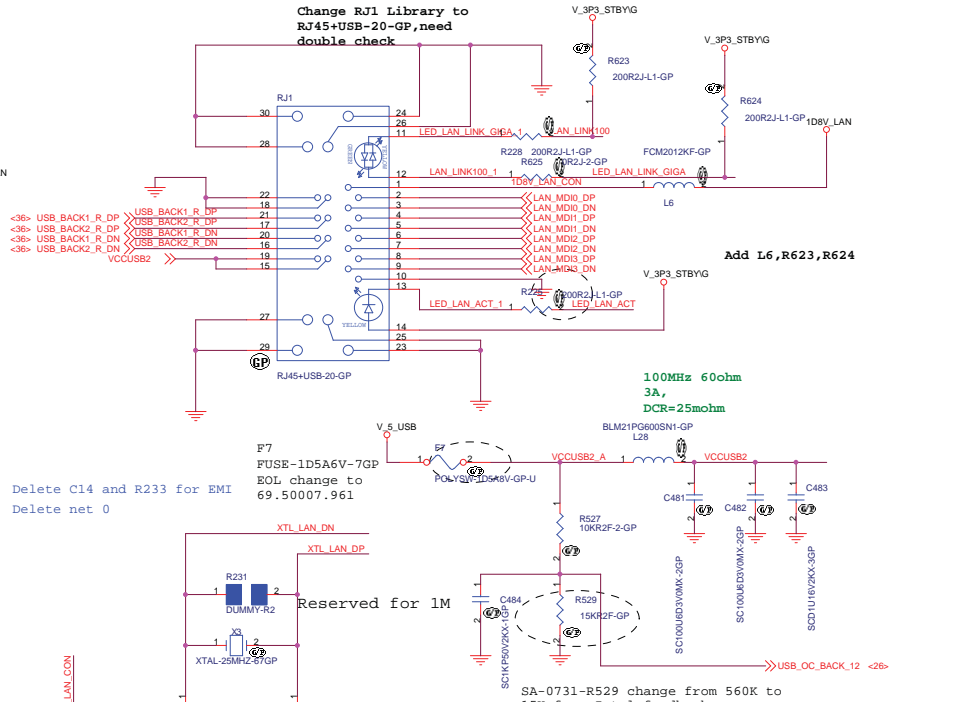
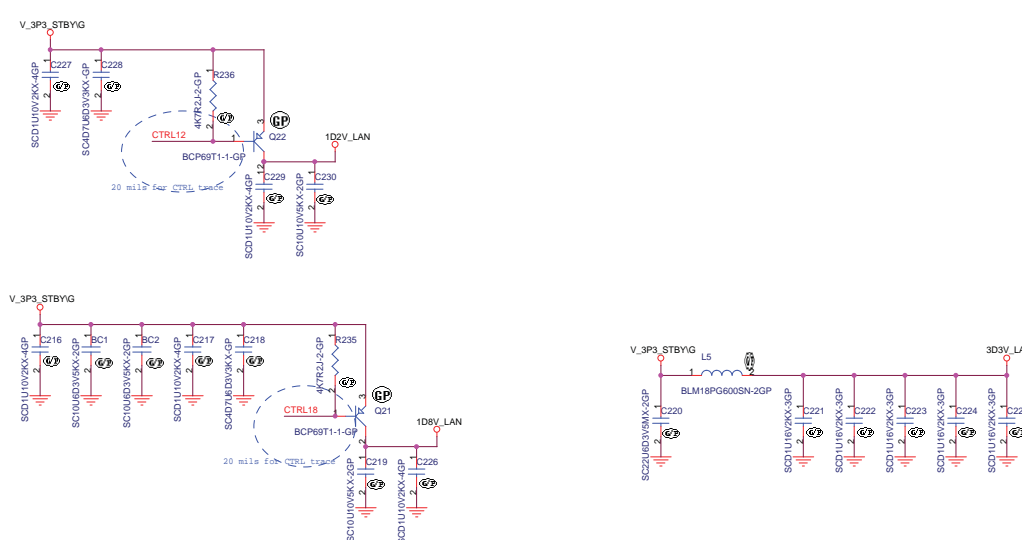
Size
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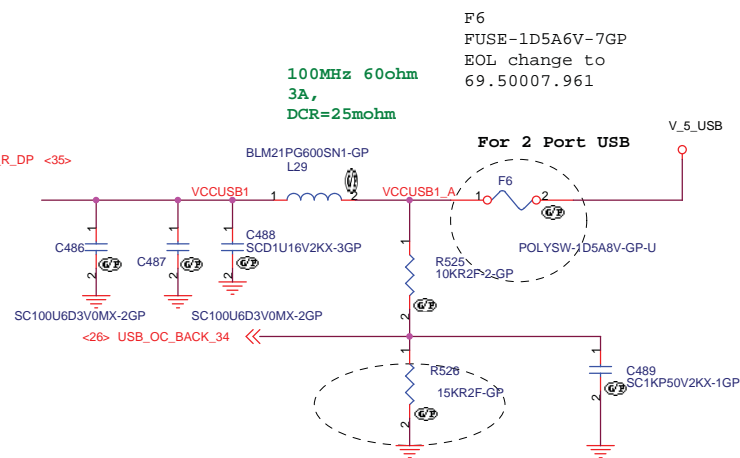
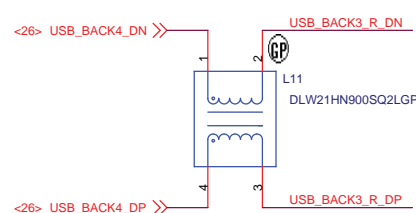
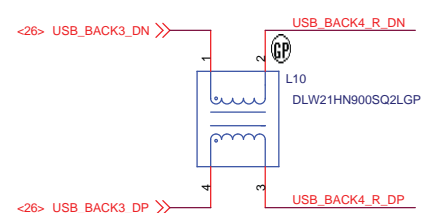
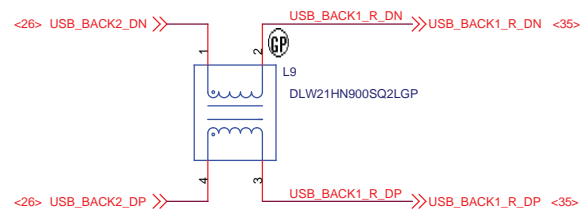
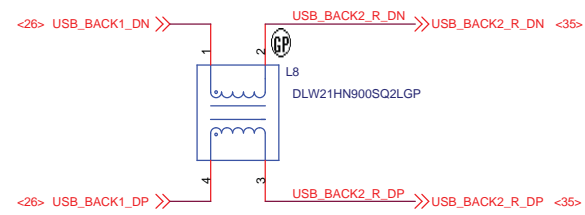
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-1

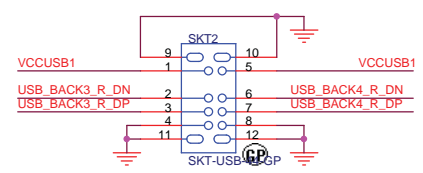
Date: Friday, December 12, 2008

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SA-0731-R526 change from 560K to 15K



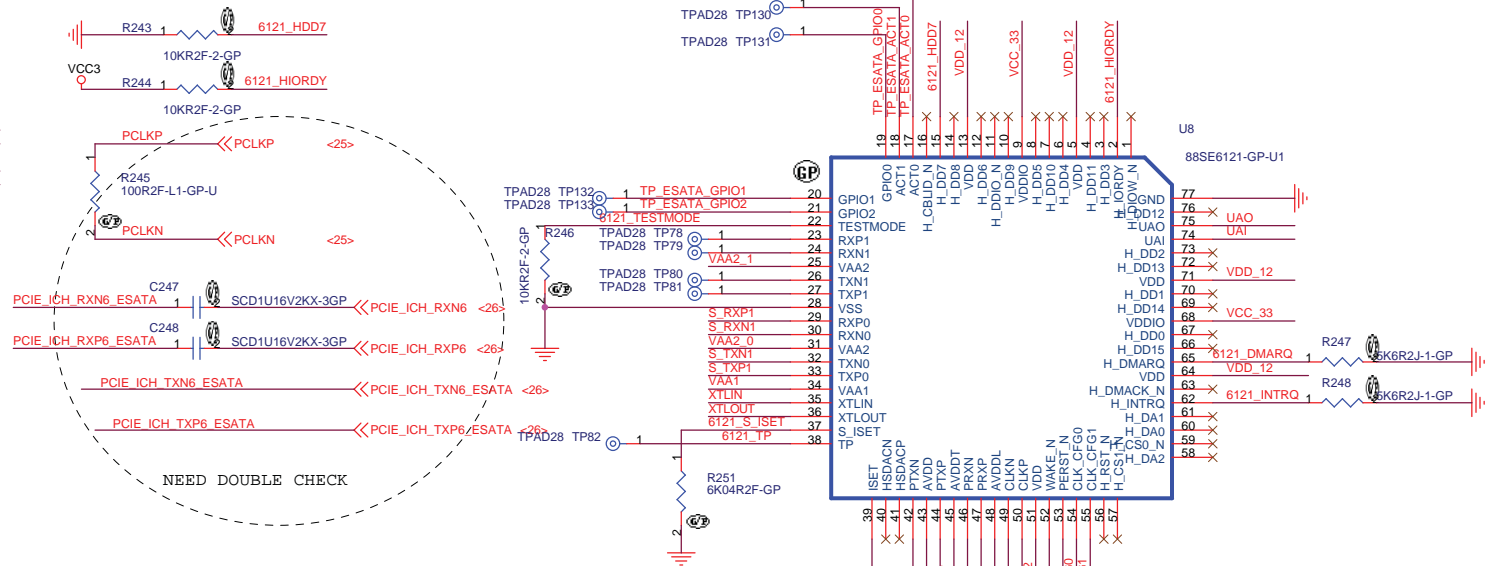
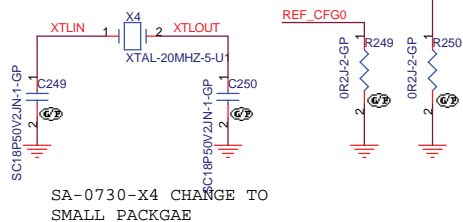
NOT SURE WHICH ONE COULD BE USED

<Variant Name>

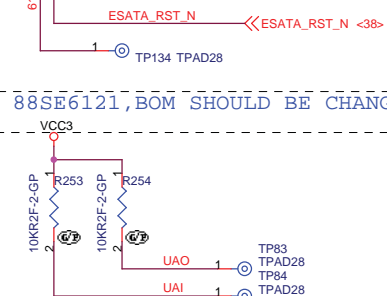
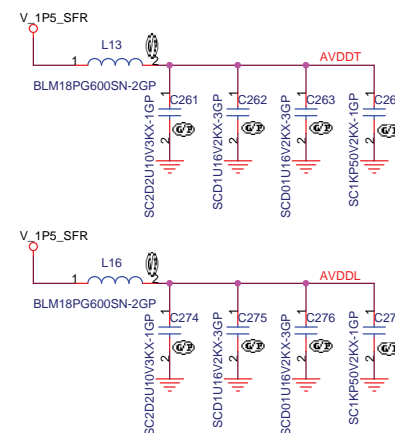
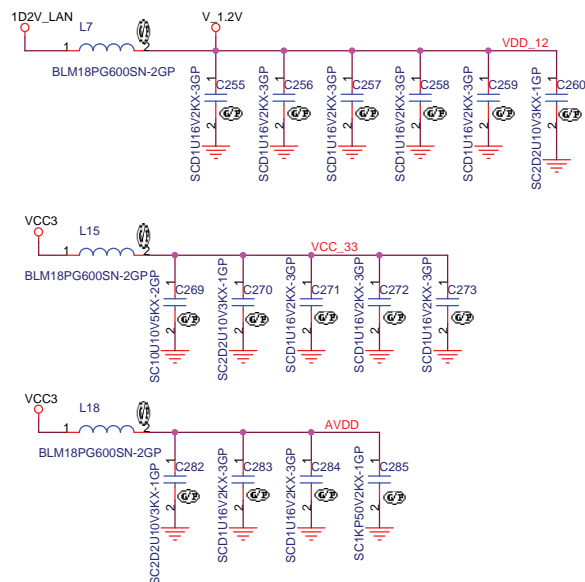
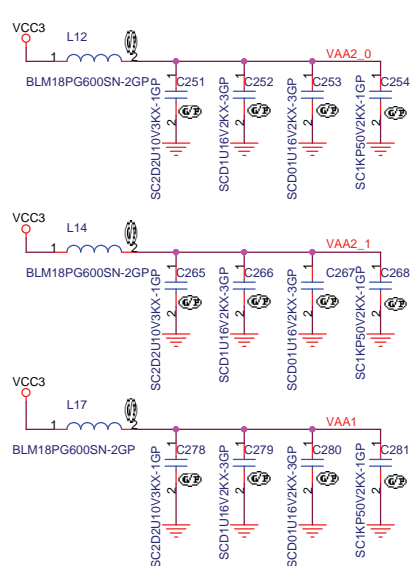
wistron

Wistron Incorporated
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Hsichih, Taipei

Title USB CONN		
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ORCAD SYMBOL IS 88SE6121,BOM SHOULD BE CHANGE
88SE6111 VCC3

SA-0804 Add R226
Dummy, and
connector to
ICH_GPIO12

delete R255,R256

SA-0804-R604 change to Dummy

reserved for pull low

2.5V I2C
inference
mount R219,R224
OPEN R227,R228

if C457 is used,vender recommend 2200pf

Add D5,R626(reserved for16.7K),C514(0.1U)
for debounce-circuit

SA-0731 delete R287
SA-0731 change R600 pin2 from net
ICH_VRMPWRGD_PU to ICH_THRM_PU_N

VR THERMAL THROTTLE CIRCUITRY

Delete R295,net
H_PROCHOT_N pull
high with R11

NET_H_FORCEPH_N
reserved for test

SUPER IO BYPASS CAP

According to SMSC5127 Anomaly
sheet,need change
the SMSC5127 0x29 register to
0x86,then the prochot will
inverter to active high to prevent
CPU throttle when booting.

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<Variant Name>

wistron

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Hsichih, Taipei

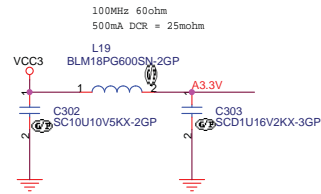
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SUPER IO SMSC5127

Size
C Document Number

Date
Friday, December 12, 2008

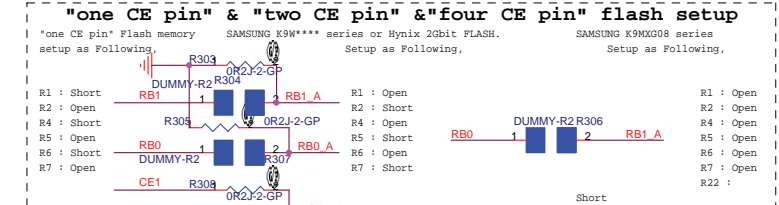
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-1

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Change NOTE-0116
Delete C14,C19,L2;change
A1.8V power source form
V_FSB_VTT to SMI321 internal
power regulator

Change NOTE-0115
Add L65 for net
A1.8V_SMI321



UNMOUNT LIST:
R752,R755,R757,R754,R759,R765,R764
L54

Interleave mode setup

R3 open : Enable
R3 short :
Disable

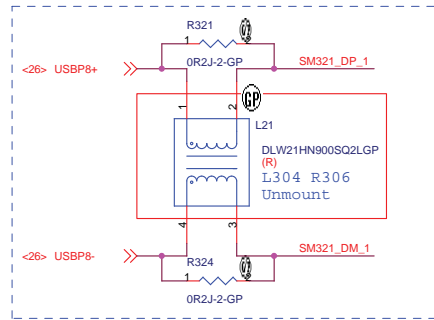
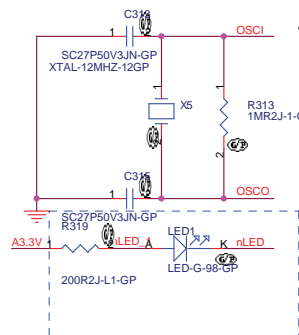


<http://hobi-elektronika.net/>

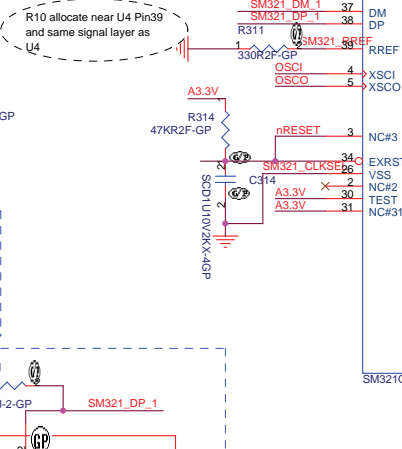
External 5V to 3.3V LDO

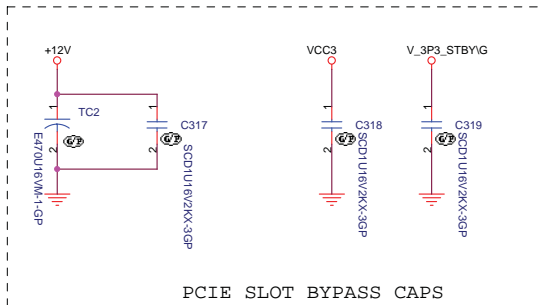
Note:
1. Use 2 pcs flash or under:
Open external LDO(U1) and short SB1.
2. Use over 2 pcs flash:
Add the external LDO(U1) and open
SB1.

Change NOTE-0115
net SM321_RV5 connect to TP
and delete R758 and C682



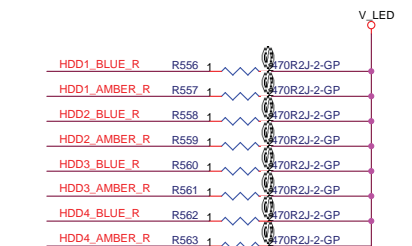
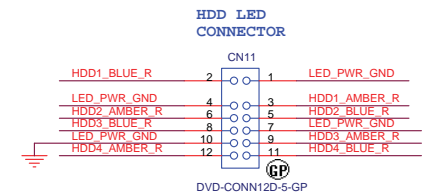
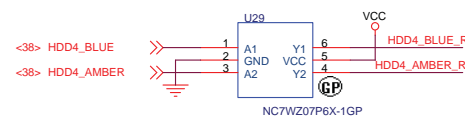
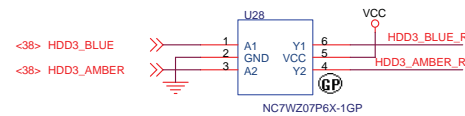
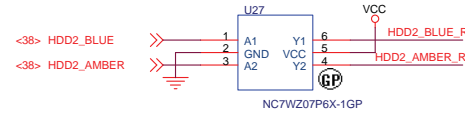
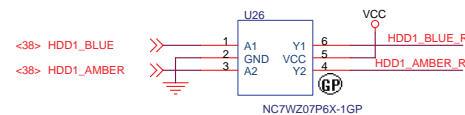
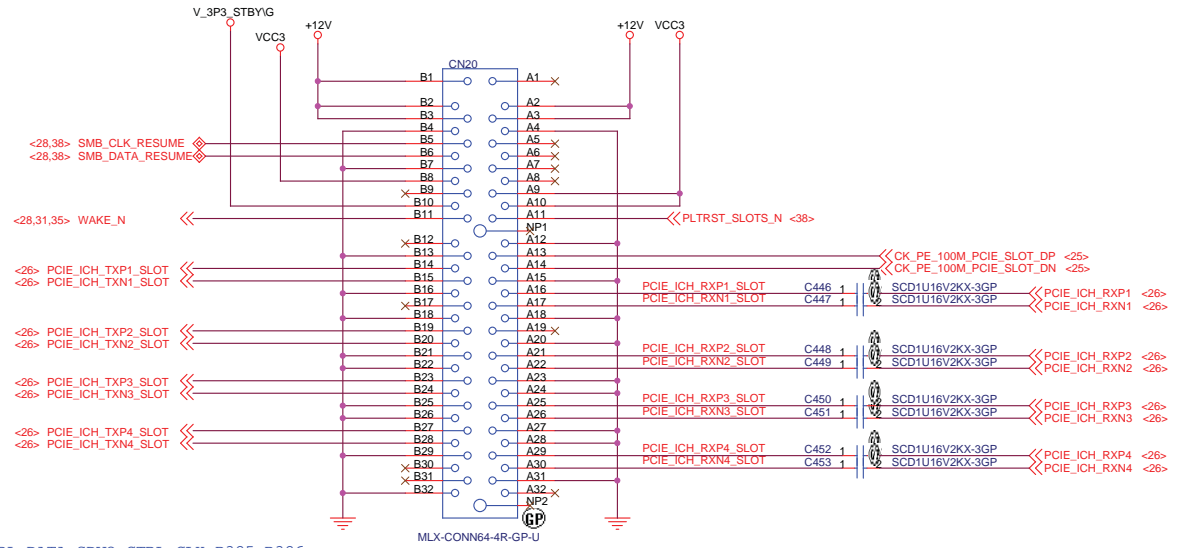
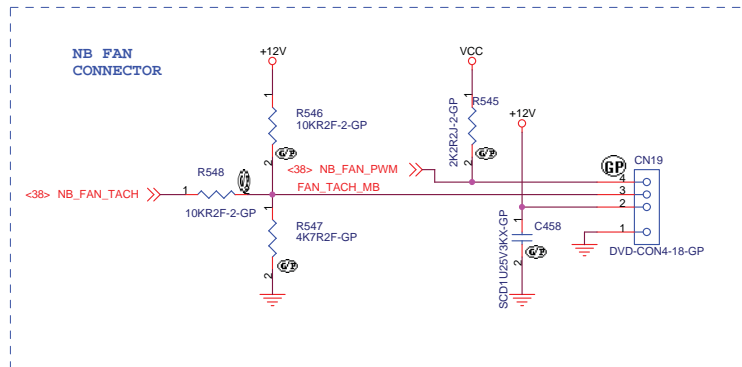
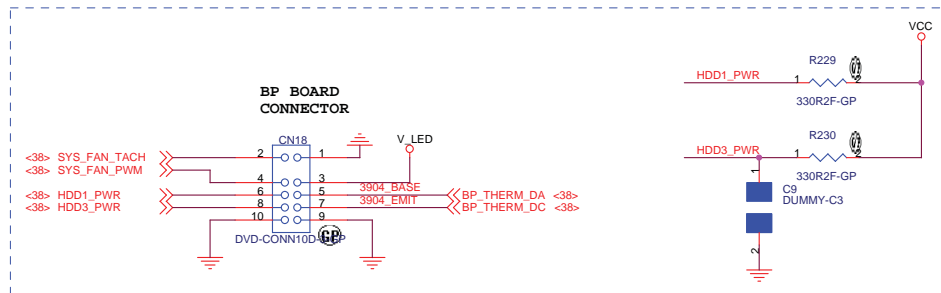
R10 allocate near U4 Pin39
and same signal layer as
U4



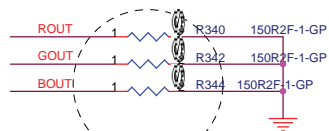
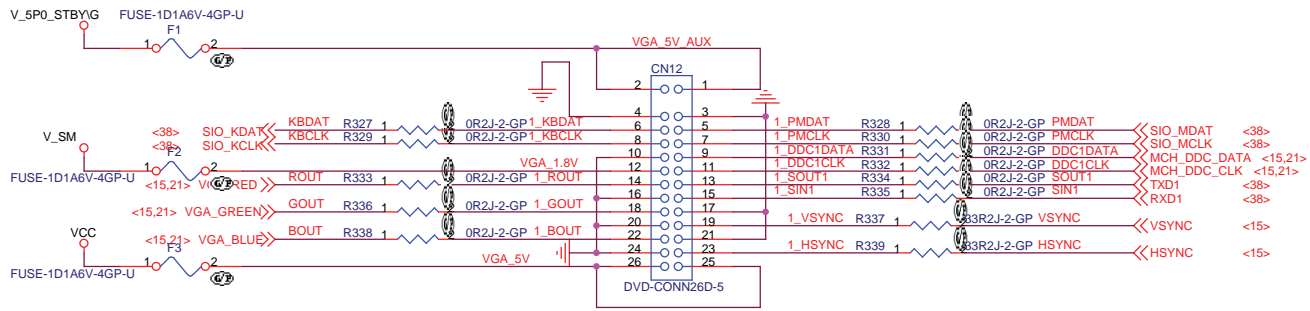
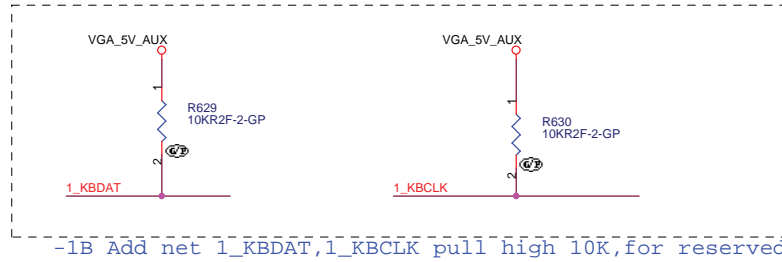


Delete R551(pull high to VCC3)-0812

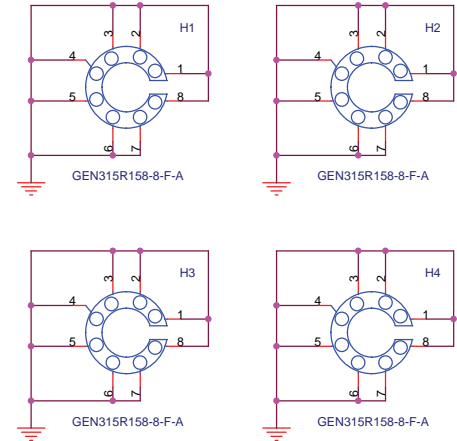
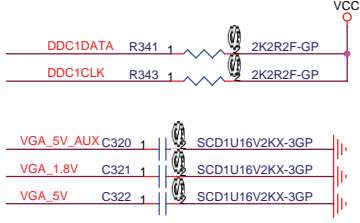
Delete net SDVO_CTRL_DATA,SDVO_CTRL_CLK,R325,R326



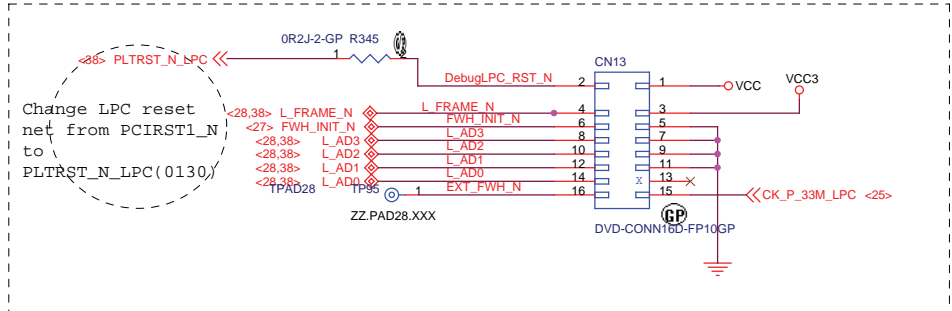
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Title		21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Size		PCIE & OTHER CONNECTOR	
A3	Document Number	S15	Rev -1
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SA-0730-change R340,R342,R344 to 150 Ohm



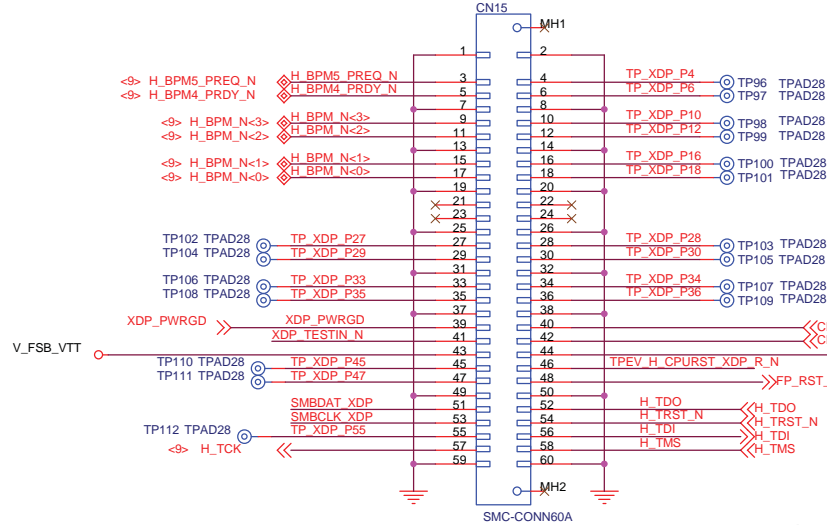
LPC Debug Port FOR MB DEBUG



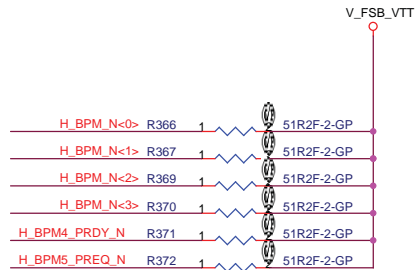
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		21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title			
DEBUG BD CONNECTOR			
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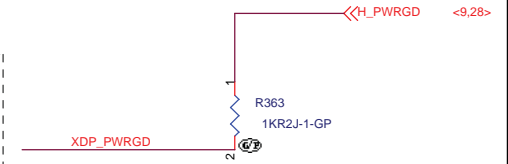
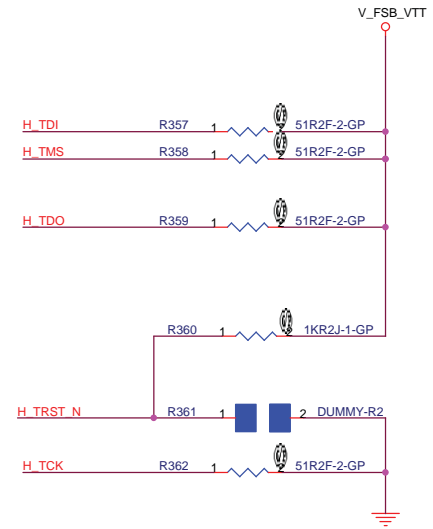
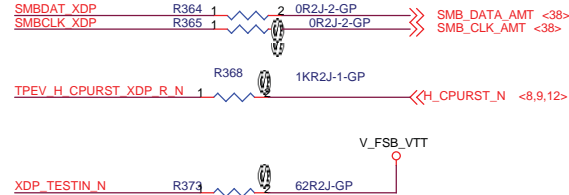
XDP For CPU



UNMOUNT LIST:



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<Variant Name>

wistron

Wistron Incorporated
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Hsichih, Taipei

Title

ITP-XDP

Size
B

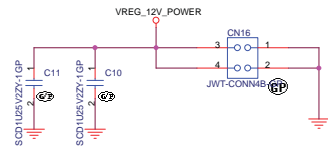
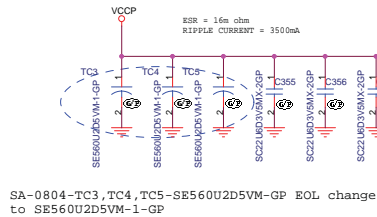
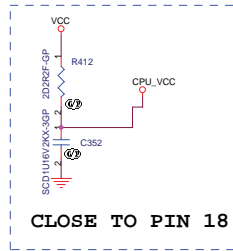
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<10> H_VID6
<10> H_VID5
<10> H_VID4
<10> H_VID3
<10> H_VID2
<10> H_VID1
<10> H_VID0



20mil trace

20mil trace

20mil trace

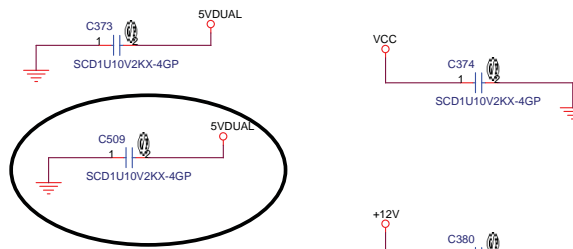
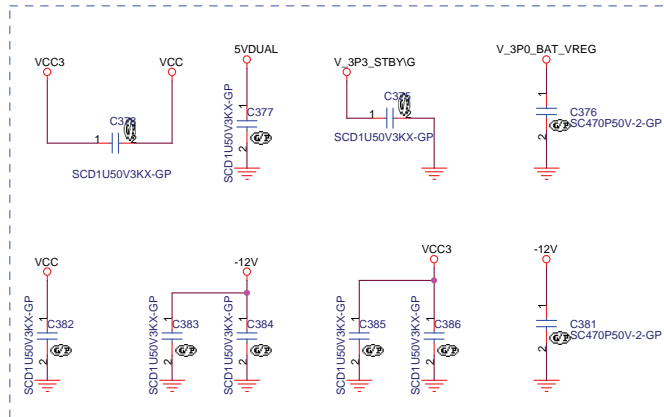
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wistron

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Hsichih, Taipei

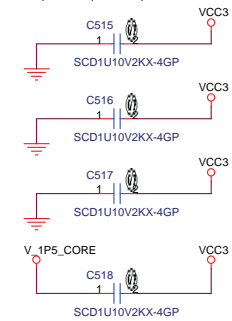
POWER VCCP VREG CONTROLLER

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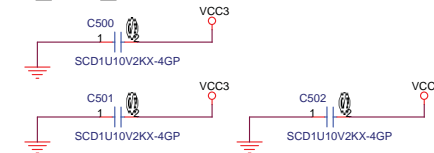
STITCHING CAPS

Add stitching caps
C515, C516, C517, C518

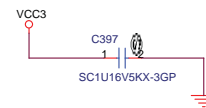


STITCHING CAPS

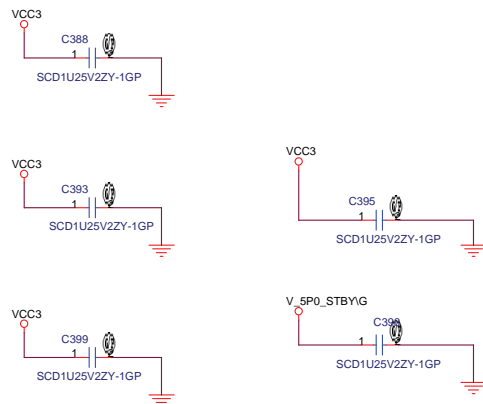
NET PCLKN, PCLKP,
MCH_DDC_CLK STITCHING CAP



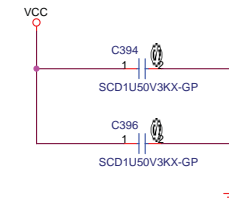
SIO STITCHING CAP



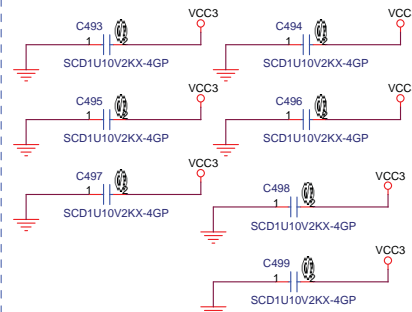
CLOCK
STITCHING CAPS



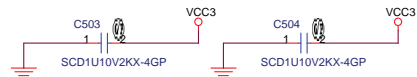
PLACE NEAR SOUTH OF
SOUTH BRIDGE



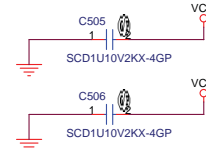
PCIE TRACE STITCHING CAP



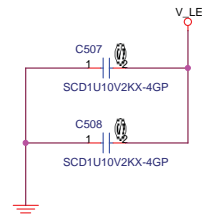
NET
CK_H_XDP_DP, CK_H_XDP_DN
STITCHING CAP



NET Vsync Hsync STITCHING CAP

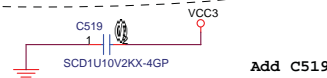


V_LED STITCHING CAP



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SA-0725-Add C493-C509 for EMI solution



Add C519

<Variant Name>

wistron

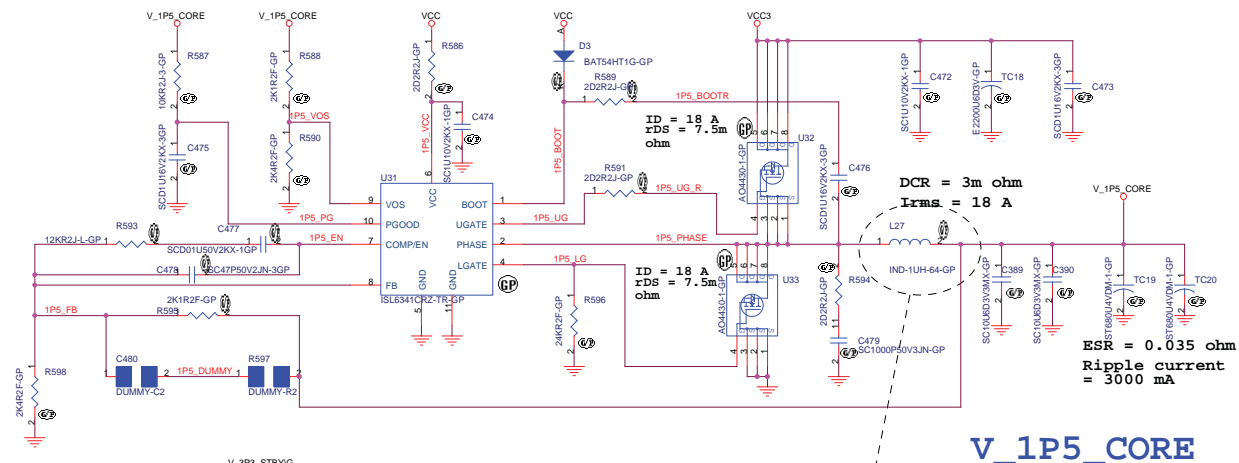
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title **POWER DECOUPLING & STITCHING**

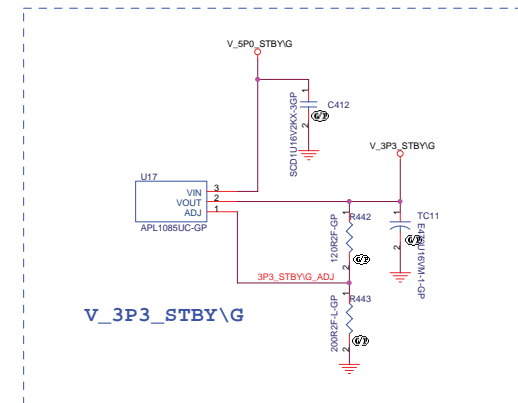
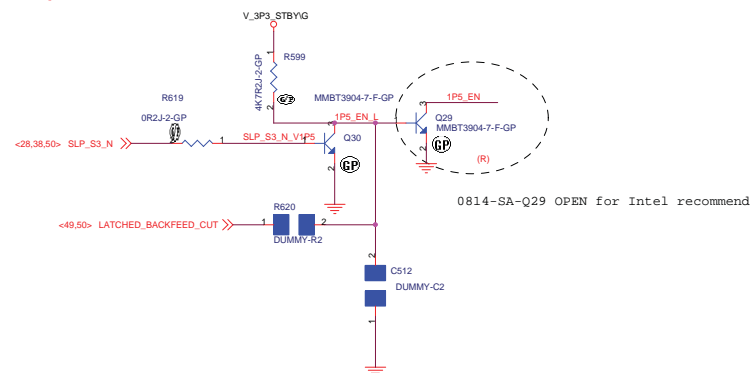
Size Document Number
Custom615

Rev
-1

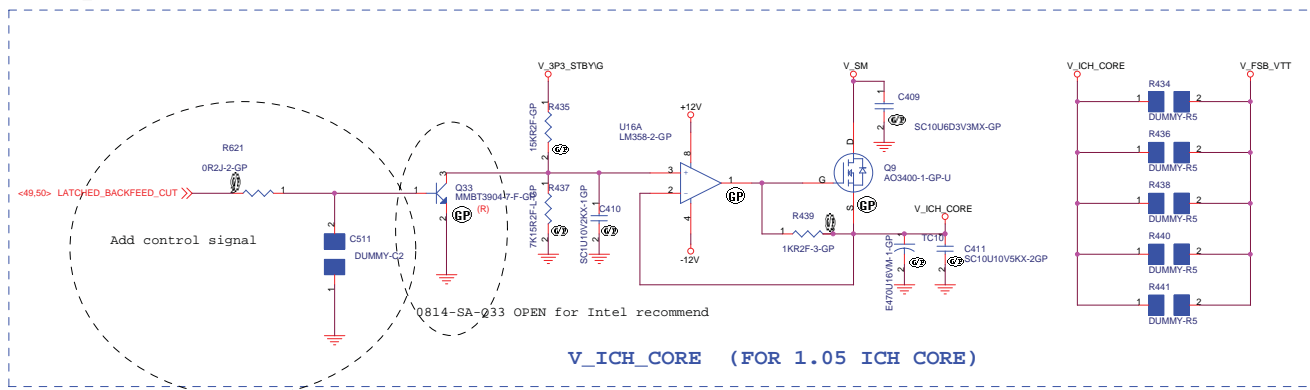
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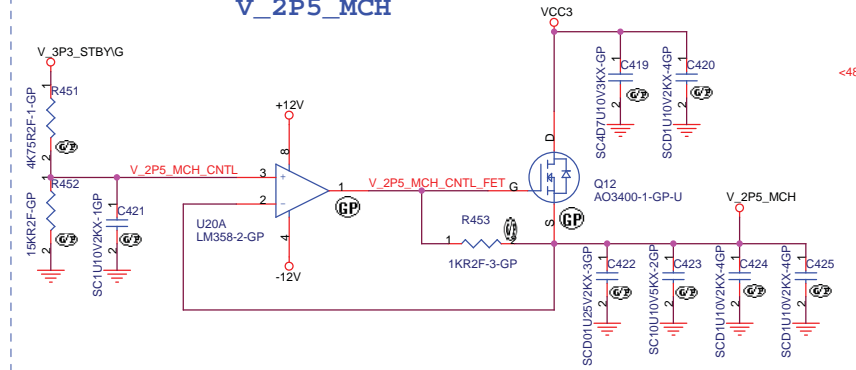
SA-0804-IND-1UH-64-GP change to
IND-1UH-41-GP-U
Because Layout Keepout issue, change back to
IND-1UH-64-GP, but BOM use IND-1UH-41-GP-U



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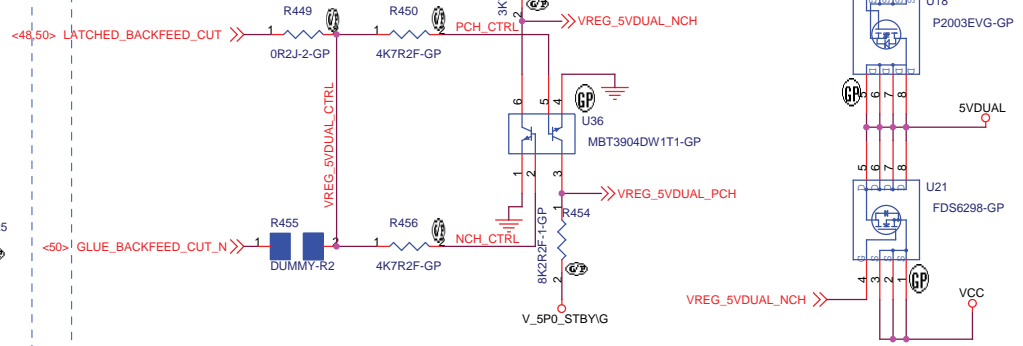
V_2P5_MCH



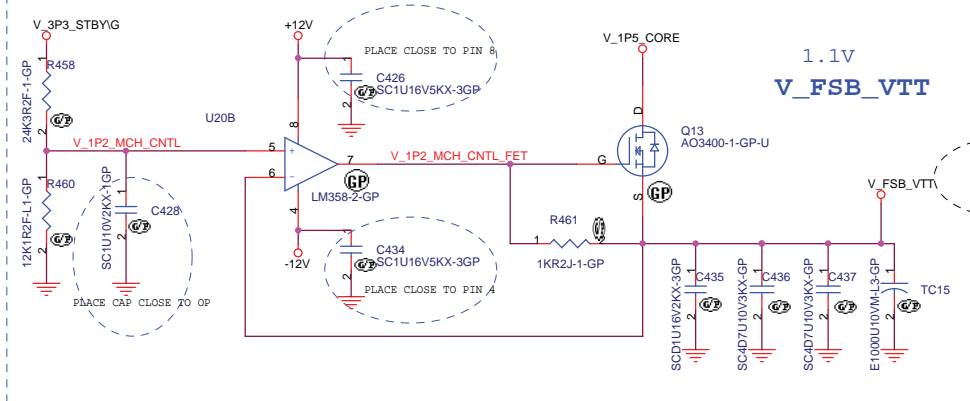
<48,50> LATCHED_BACKFEED_CUT

<50> GLUE_BACKFEED_CUT_N

5VDUAL VR

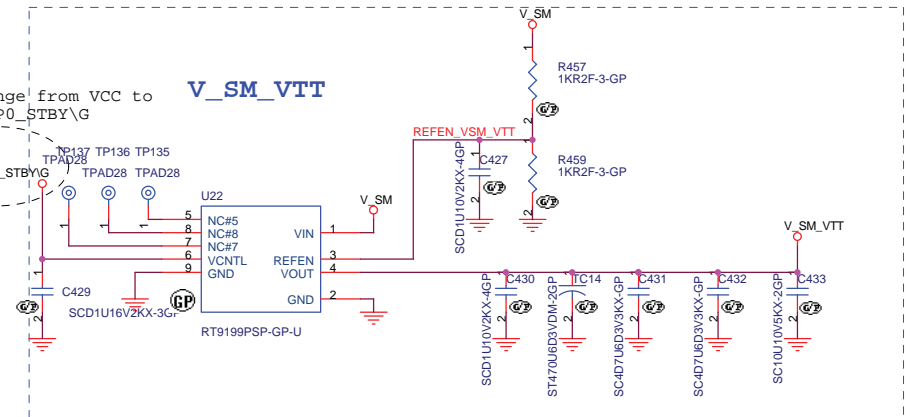


1.1V V_FSB_VTT

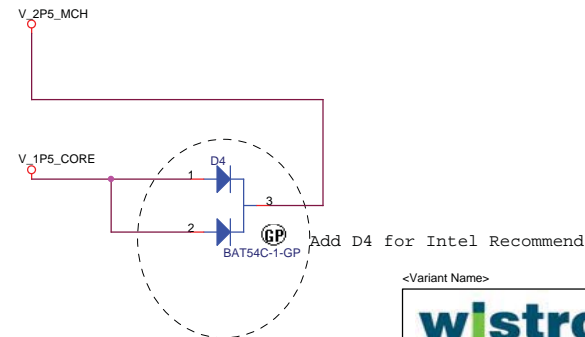


V_SM_VTT

change from VCC to
V_5P0_STBYG



Delete V_5_USB control circuit and
connect to 5VDUAL directly



<Variant Name>

wistron

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Hsichih, Taipei

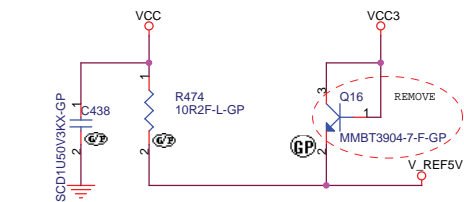
Title
POWER VTT 5VDUAL 2P5_MCH

Size Document Number
CustomS15

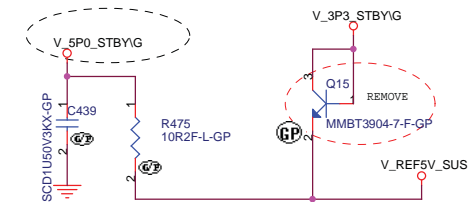
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-1

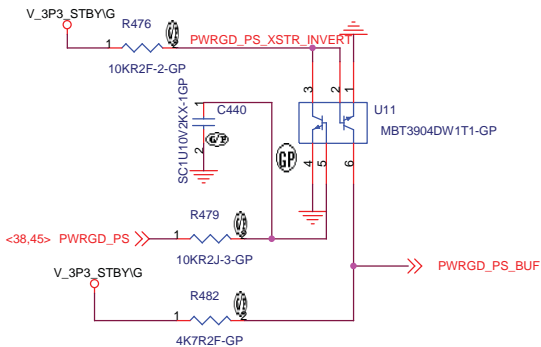
PLACE REF5V CIRCUITRY NEAR ICH



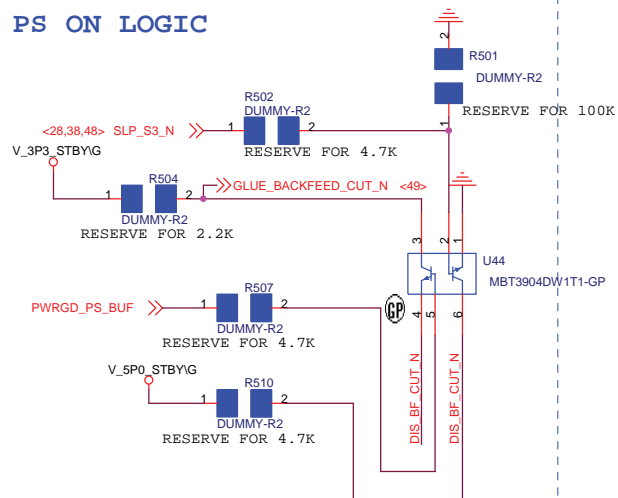
REF5V_SUS



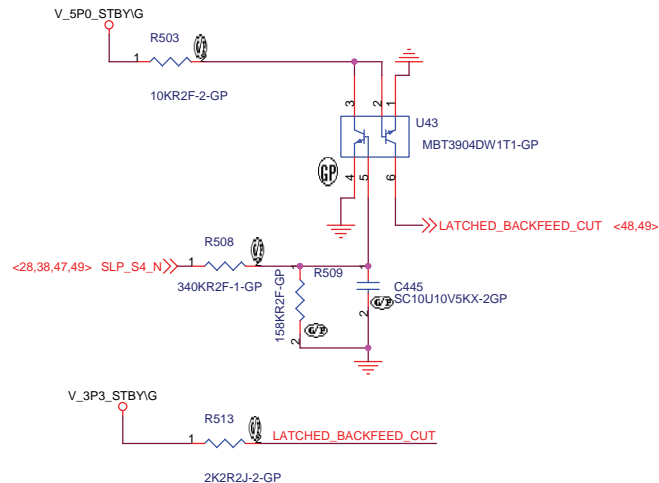
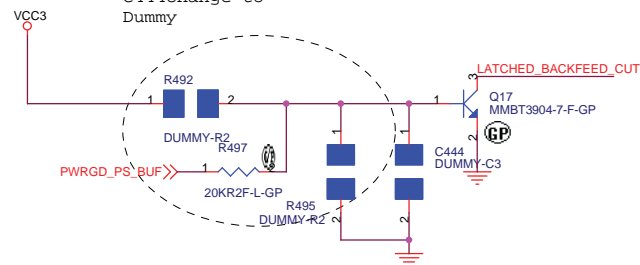
change C439 & R475 power source from VCC to V_5P0_STBY\G




PS ON LOGIC



R492,R495,
C444change to
Dummy



<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
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