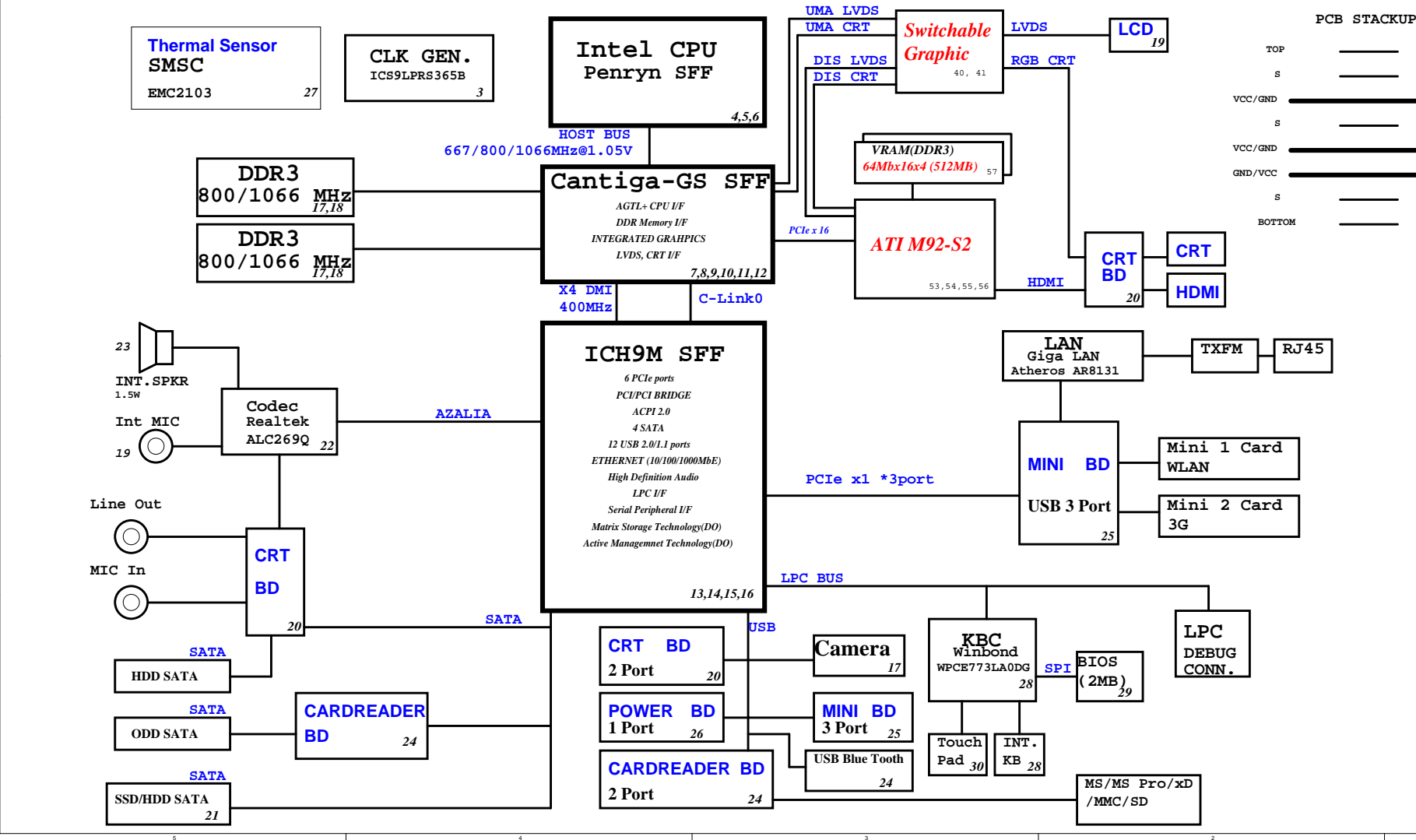


JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SB
REVISION : 08274-1



SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
5V_S5(6A)	3D3V_S5(5A)
5V_AUX_S5	3D3V_AUX_S5
DCBATOUT	
RT8202 37	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)
RT8202 38	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)
RT9026 39	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3(1.2A)
CHARGER MAX8731A 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3207A 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A
VGA ISL6263A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE (7A)

PCB STACKUP		
TOP	_____	L1
S	_____	L2
VCC/GND	_____	L3
S	_____	L4
VCC/GND	_____	L5
GND/VCC	_____	L6
S	_____	L7
BOTTOM	_____	L8

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File

BLOCK DIAGRAM

Size Custom

Document Number

JM41 Discrete

Rev -1

Date: Tuesday, April 07, 2009

Sheet 1 of 48

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

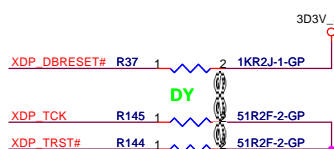
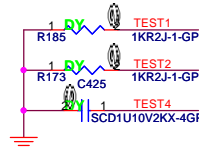
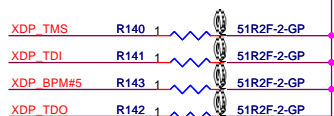
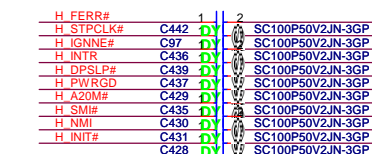
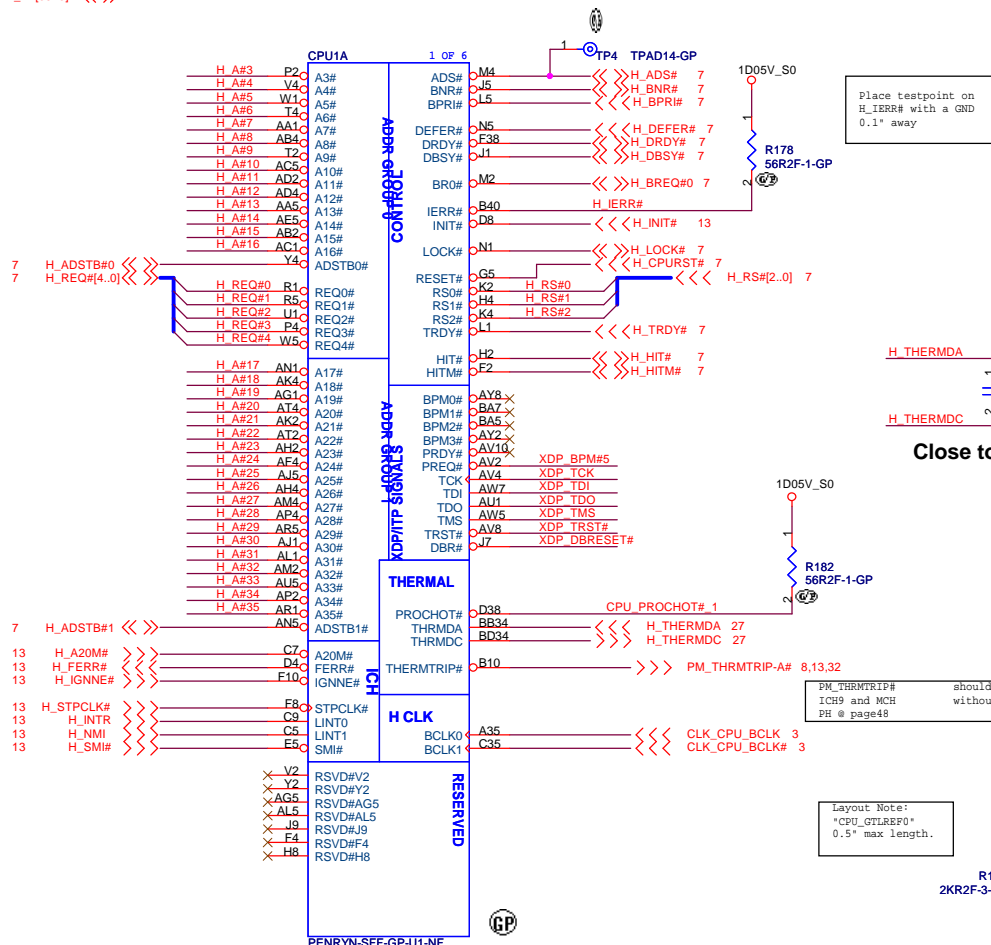
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

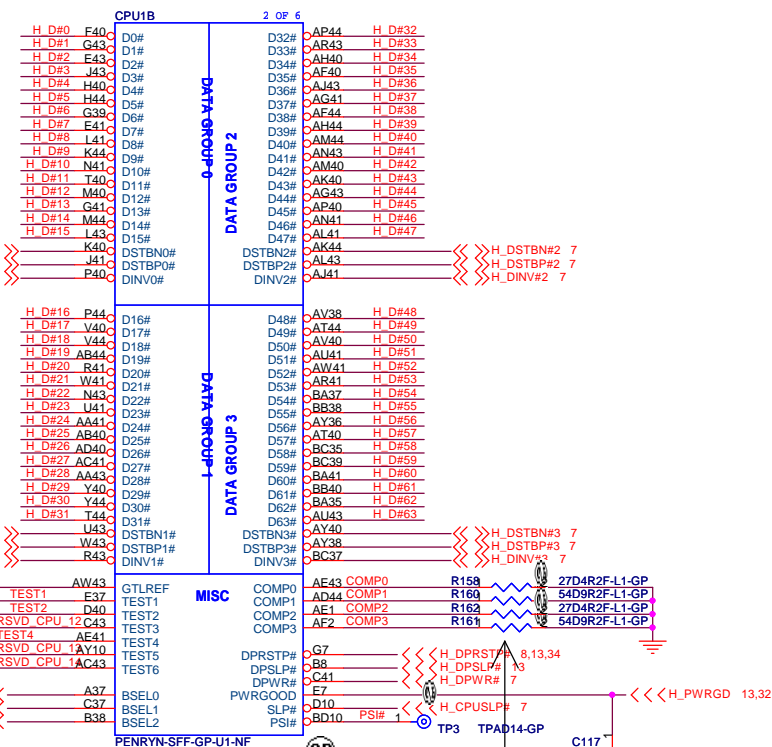
Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCie are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

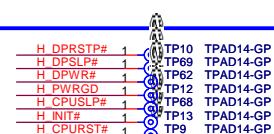
NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.



All place within 2" to CPU



Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals



Place these TP on button-side,
easy to measure.

```
H_DINV#[3..0] << >> H_DINV#[3..0] 7
H_DSTBN#[3..0] << >> H_DSTBN#[3..0] 7
H_DSTBP#[3..0] << >> H_DSTBP#[3..0] 7
H_D#[63..0] << >> H_D#[63..0] 7
```

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5" .

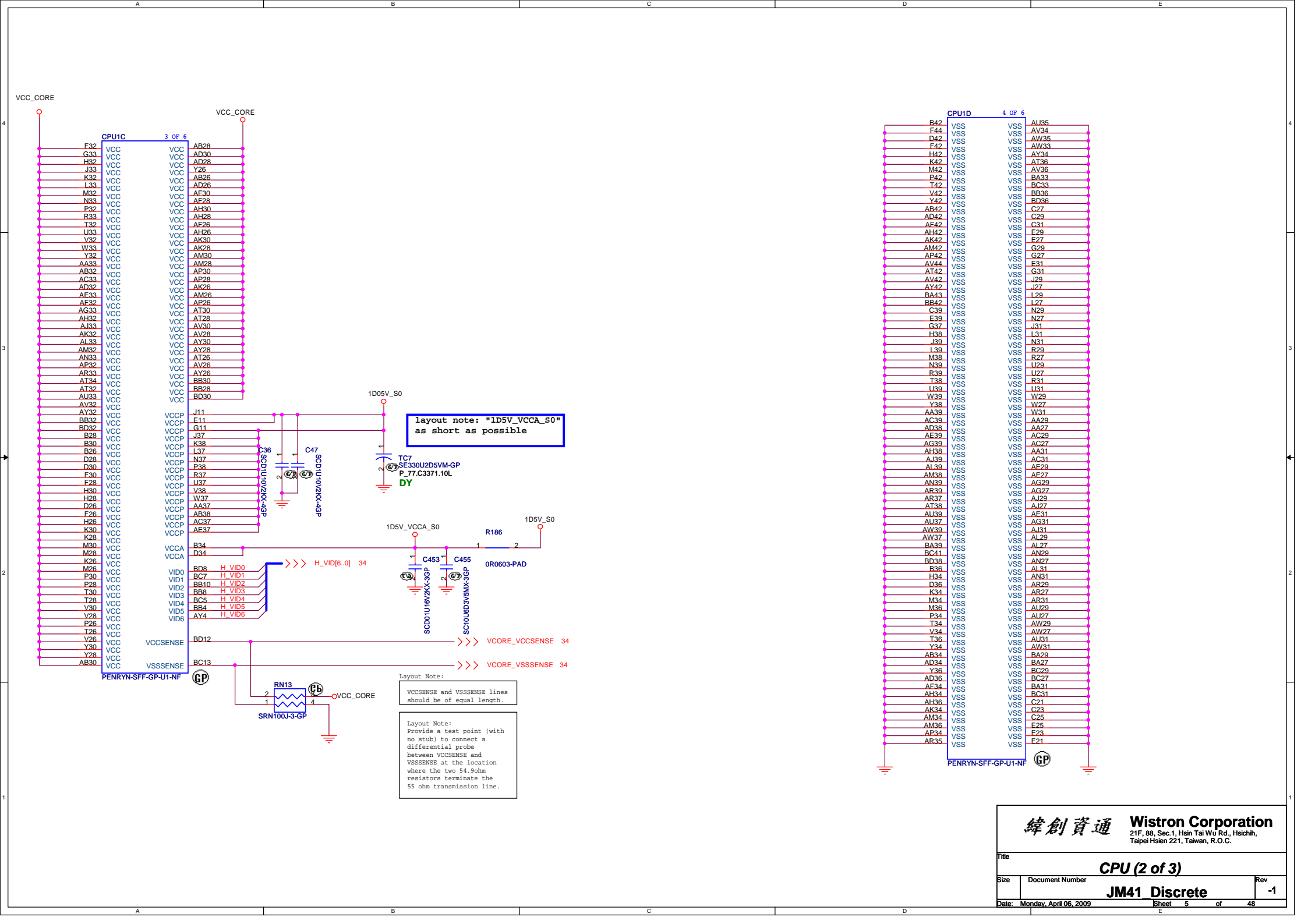
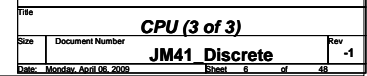
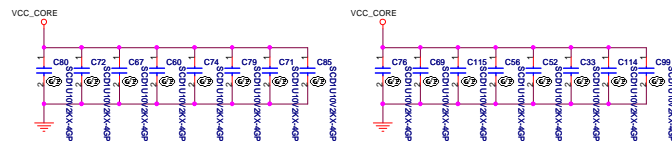
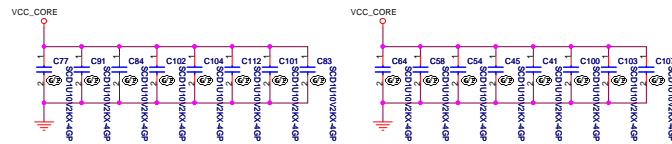
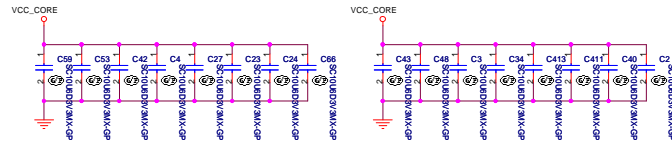
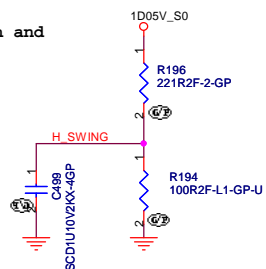


Figure 1 shows two schematic diagrams of 10-bit DACs. Diagram (a) is a 10-bit DAC with 10 resistors (C416 to C5) and 10 capacitors (C1 to C9). Diagram (b) is a 10-bit DAC with 10 resistors (C412 to C5) and 10 capacitors (C19 to C9). Both diagrams show a VCC_CORE supply connected to a network of resistors and capacitors, which are then connected to a common output node.

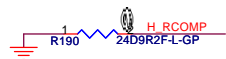


H_SWING routing Trace width and Spacing use 10 / 20 mil

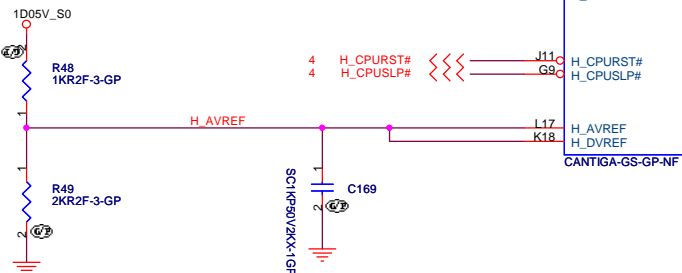
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



NB1A			1 OF 10		
H_D#0	J7	H_D#_0	H_A#_3	L15	H_A#3
H_D#1	H6	H_D#_1	H_A#_4	B14	H_A#4
H_D#2	L11	H_D#_2	H_A#_5	C15	H_A#5
H_D#3	J3	H_D#_3	H_A#_6	D12	H_A#6
H_D#4	H4	H_D#_4	H_A#_7	F14	H_A#7
H_D#5	G3	H_D#_5	H_A#_8	G17	H_A#8
H_D#6	K10	H_D#_6	H_A#_9	B12	H_A#9
H_D#7	K12	H_D#_7	H_A#_10	J15	H_A#10
H_D#8	L1	H_D#_8	H_A#_11	D16	H_A#11
H_D#9	M10	H_D#_9	H_A#_12	C17	H_A#12
H_D#10	M6	H_D#_10	H_A#_13	D14	H_A#13
H_D#11	N11	H_D#_11	H_A#_14	K16	H_A#14
H_D#12	L7	H_D#_12	H_A#_15	F16	H_A#15
H_D#13	K6	H_D#_13	H_A#_16	B16	H_A#16
H_D#14	M4	H_D#_14	H_A#_17	C21	H_A#17
H_D#15	K4	H_D#_15	H_A#_18	D18	H_A#18
H_D#16	P6	H_D#_16	H_A#_19	J19	H_A#19
H_D#17	W9	H_D#_17	H_A#_20	J21	H_A#20
H_D#18	V6	H_D#_18	H_A#_21	B18	H_A#21
H_D#19	V2	H_D#_19	H_A#_22	D22	H_A#22
H_D#20	P10	H_D#_20	H_A#_23	G19	H_A#23
H_D#21	W7	H_D#_21	H_A#_24	J17	H_A#24
H_D#22	N9	H_D#_22	H_A#_25	L21	H_A#25
H_D#23	P4	H_D#_23	H_A#_26	L19	H_A#26
H_D#24	U9	H_D#_24	H_A#_27	G21	H_A#27
H_D#25	V4	H_D#_25	H_A#_28	D20	H_A#28
H_D#26	U1	H_D#_26	H_A#_29	K22	H_A#29
H_D#27	W3	H_D#_27	H_A#_30	F18	H_A#30
H_D#28	V10	H_D#_28	H_A#_31	K20	H_A#31
H_D#29	U7	H_D#_29	H_A#_32	F20	H_A#32
H_D#30	W11	H_D#_30	H_A#_33	F22	H_A#33
H_D#31	U11	H_D#_31	H_A#_34	B20	H_A#34
H_D#32	AC11	H_D#_32	H_A#_35	A19	H_A#35
H_D#33	AC9	H_D#_33			
H_D#34	Y4	H_D#_34			
H_D#35	Y10	H_D#_35			
H_D#36	AB6	H_D#_36			
H_D#37	AA9	H_D#_37			
H_D#38	AB10	H_D#_38			
H_D#39	AA1	H_D#_39			
H_D#40	AC3	H_D#_40			
H_D#41	AC7	H_D#_41			
H_D#42	AD12	H_D#_42			
H_D#43	AB4	H_D#_43			
H_D#44	Y6	H_D#_44			
H_D#45	AD10	H_D#_45			
H_D#46	AA11	H_D#_46			
H_D#47	AB2	H_D#_47			
H_D#48	AD4	H_D#_48			
H_D#49	AE7	H_D#_49			
H_D#50	AD2	H_D#_50			
H_D#51	AD6	H_D#_51			
H_D#52	AE3	H_D#_52			
H_D#53	AG9	H_D#_53			
H_D#54	AG7	H_D#_54			
H_D#55	AE11	H_D#_55			
H_D#56	AK6	H_D#_56			
H_D#57	AF6	H_D#_57			
H_D#58	AJ9	H_D#_58			
H_D#59	AH6	H_D#_59			
H_D#60	AE12	H_D#_60			
H_D#61	AH4	H_D#_61			
H_D#62	AJ7	H_D#_62			
H_D#63	AE9	H_D#_63			

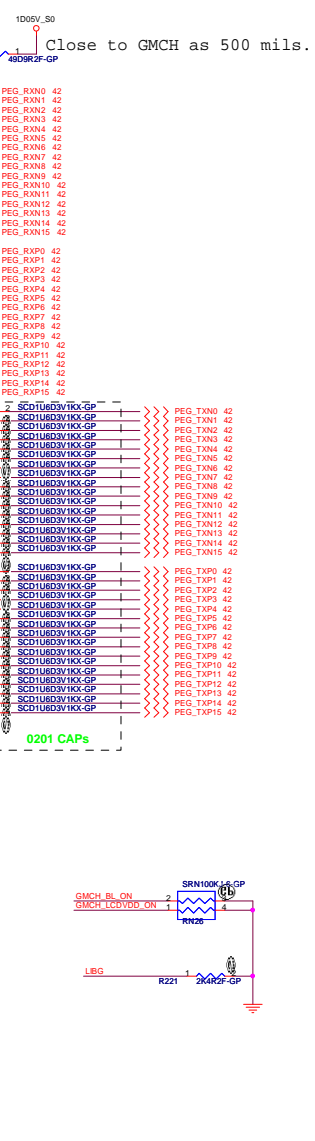
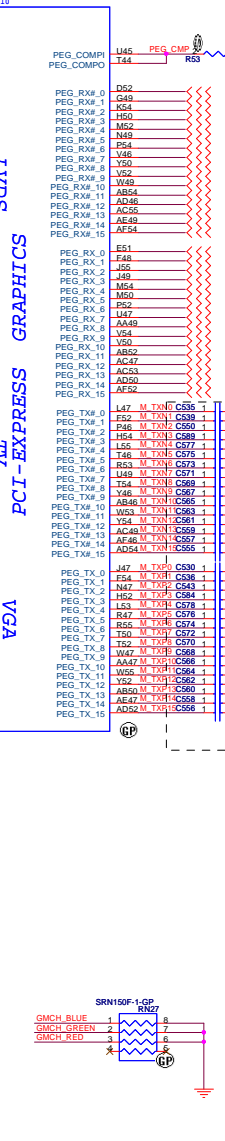
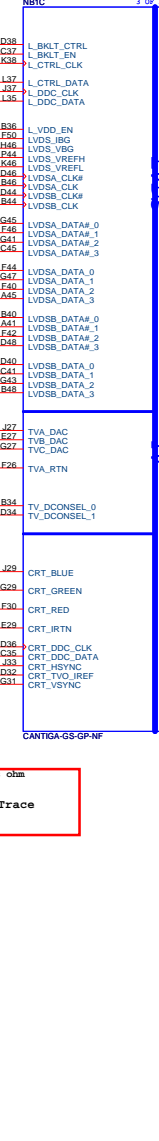
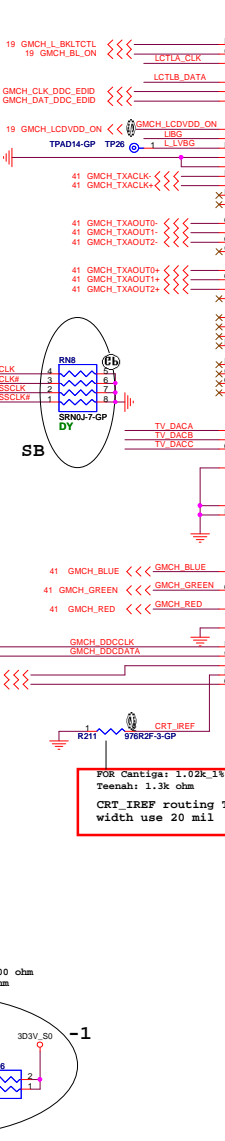
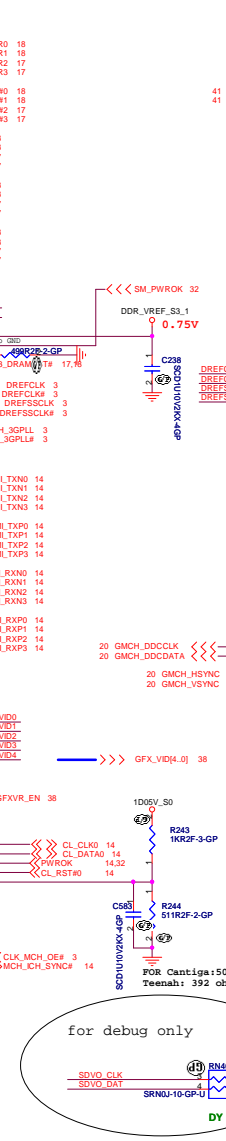
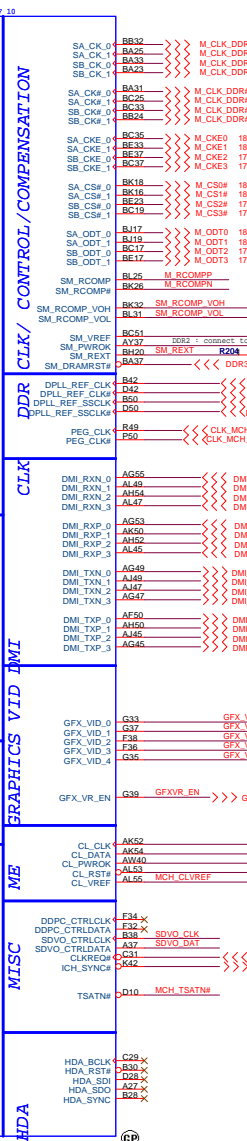
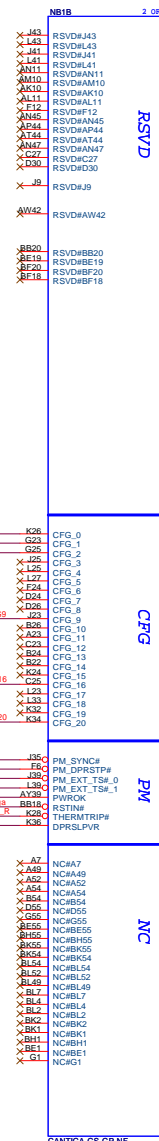
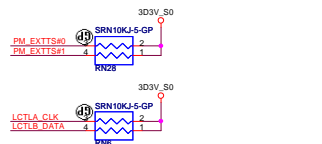
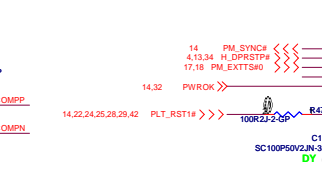
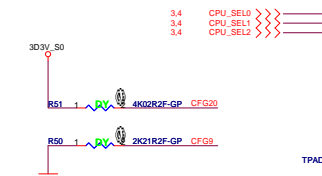
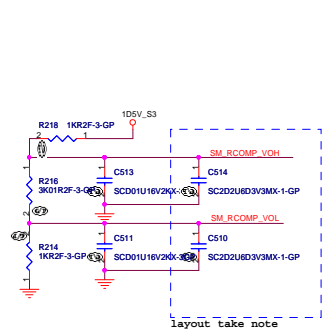
HOST

H_A#_3	L15	H_A#3	H_A#[35..3]	<<<>>>H_A#[35..3]	4
H_A#_4	B14	H_A#4			
H_A#_5	C15	H_A#5			
H_A#_6	D12	H_A#6			
H_A#_7	F14	H_A#7			
H_A#_8	G17	H_A#8			
H_A#_9	B12	H_A#9			
H_A#_10	J15	H_A#10			
H_A#_11	D16	H_A#11			
H_A#_12	C17	H_A#12			
H_A#_13	D14	H_A#13			
H_A#_14	K16	H_A#14			
H_A#_15	F16	H_A#15			
H_A#_16	B16	H_A#16			
H_A#_17	C21	H_A#17			
H_A#_18	D18	H_A#18			
H_A#_19	J19	H_A#19			
H_A#_20	J21	H_A#20			
H_A#_21	B18	H_A#21			
H_A#_22	D22	H_A#22			
H_A#_23	G19	H_A#23			
H_A#_24	J17	H_A#24			
H_A#_25	L21	H_A#25			
H_A#_26	L19	H_A#26			
H_A#_27	G21	H_A#27			
H_A#_28	D20	H_A#28			
H_A#_29	K22	H_A#29			
H_A#_30	F18	H_A#30			
H_A#_31	K20	H_A#31			
H_A#_32	F20	H_A#32			
H_A#_33	F22	H_A#33			
H_A#_34	B20	H_A#34			
H_A#_35	A19	H_A#35			
H_ADS#	F10	H_ADS#	<<<>>>H_ADS#	4	
H_ADSTB#_0	A15	H_ADSTB#0	<<<>>>H_ADSTB#0	4	
H_ADSTB#_1	C19	H_ADSTB#1	<<<>>>H_ADSTB#1	4	
H_BNR#	C9	H_BNR#	<<<>>>H_BNR#	4	
H_BPRI#	B8	H_BPRI#	<<<>>>H_BPRI#	4	
H_BREQ#	C11	H_BREQ#	<<<>>>H_BREQ#	4	
H_DEFER#	E5	H_DEFER#	<<<>>>H_DEFER#	4	
H_DBSY#	D6	H_DBSY#	<<<>>>H_DBSY#	4	
H_DBSY#	AH10	H_DBSY#	<<<>>>H_DBSY#	4	
HPLL_CLK#	AJ11	CLK_MCH_BCLK#	<<<>>>CLK_MCH_BCLK#	3	
HPLL_CLK#	AJ11	CLK_MCH_BCLK#	<<<>>>CLK_MCH_BCLK#	3	
H_DPWR#	G11	H_DPWR#	<<<>>>H_DPWR#	4	
H_DRDY#	H2	H_DRDY#	<<<>>>H_DRDY#	4	
H_HIT#	C7	H_HIT#	<<<>>>H_HIT#	4	
H_HITM#	E8	H_HITM#	<<<>>>H_HITM#	4	
H_LOCK#	A11	H_LOCK#	<<<>>>H_LOCK#	4	
H_TRDY#	D8	H_TRDY#	<<<>>>H_TRDY#	4	
H_DINV#_0	L9	H_DINV#0	H_DINV#[3..0]	<<<>>>H_DINV#[3..0]	4
H_DINV#_1	N7	H_DINV#1			
H_DINV#_2	AA7	H_DINV#2			
H_DINV#_3	AG3	H_DINV#3			
H_DSTBN#_0	K2	H_DSTBN#0	H_DSTBN#[3..0]	<<<>>>H_DSTBN#[3..0]	4
H_DSTBN#_1	N3	H_DSTBN#1			
H_DSTBN#_2	AA3	H_DSTBN#2			
H_DSTBN#_3	AE4	H_DSTBN#3			
H_DSTBP#_0	L3	H_DSTBP#0	H_DSTBP#[3..0]	<<<>>>H_DSTBP#[3..0]	4
H_DSTBP#_1	M2	H_DSTBP#1			
H_DSTBP#_2	Y2	H_DSTBP#2			
H_DSTBP#_3	AE2	H_DSTBP#3			
H_REQ#_0	J13	H_REQ#0	<<<>>>H_REQ#[4..0]	4	
H_REQ#_1	L13	H_REQ#1			
H_REQ#_2	C13	H_REQ#2			
H_REQ#_3	G13	H_REQ#3			
H_REQ#_4	G15	H_REQ#4			
H_RS#_0	F4	H_RS#0	>>>>H_RS#[2..0]	4	
H_RS#_1	F2	H_RS#1			
H_RS#_2	G7	H_RS#2			

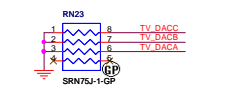
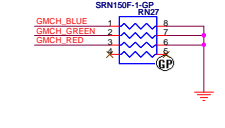
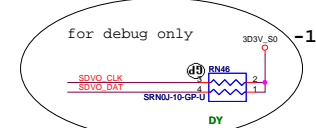
DIS

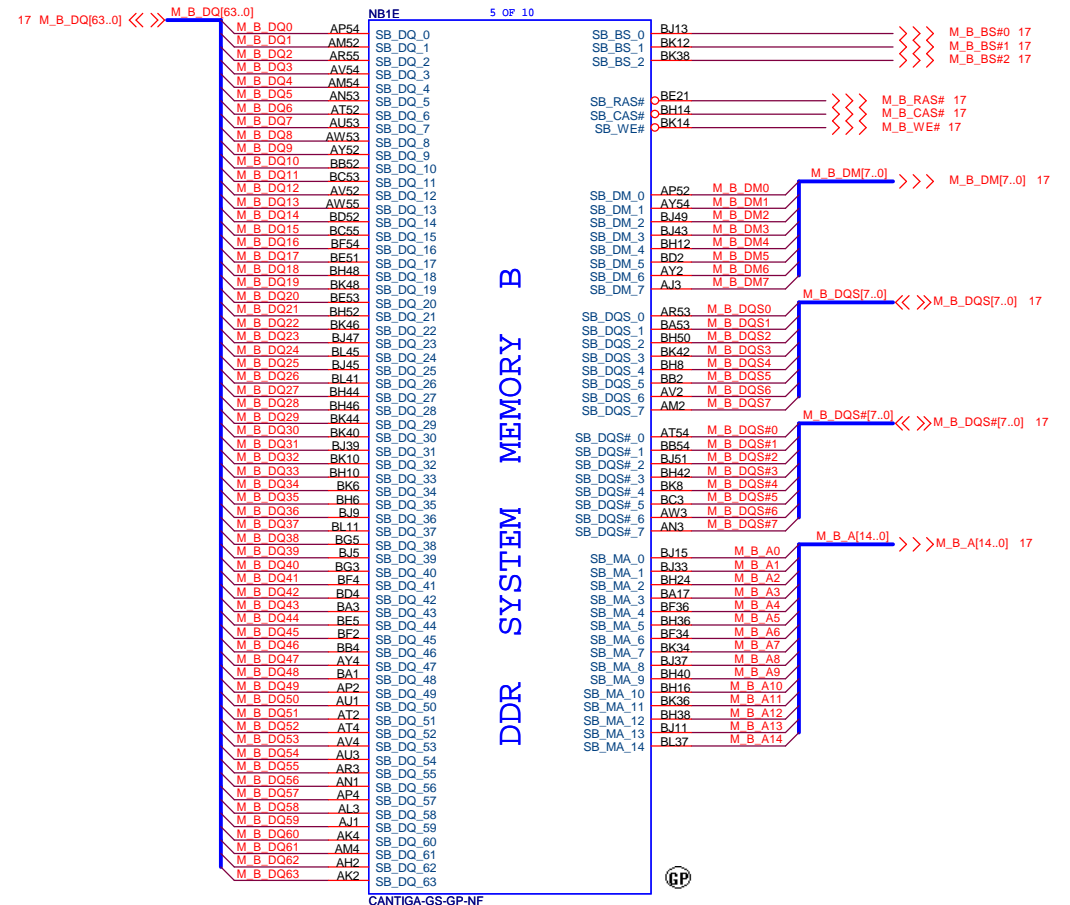
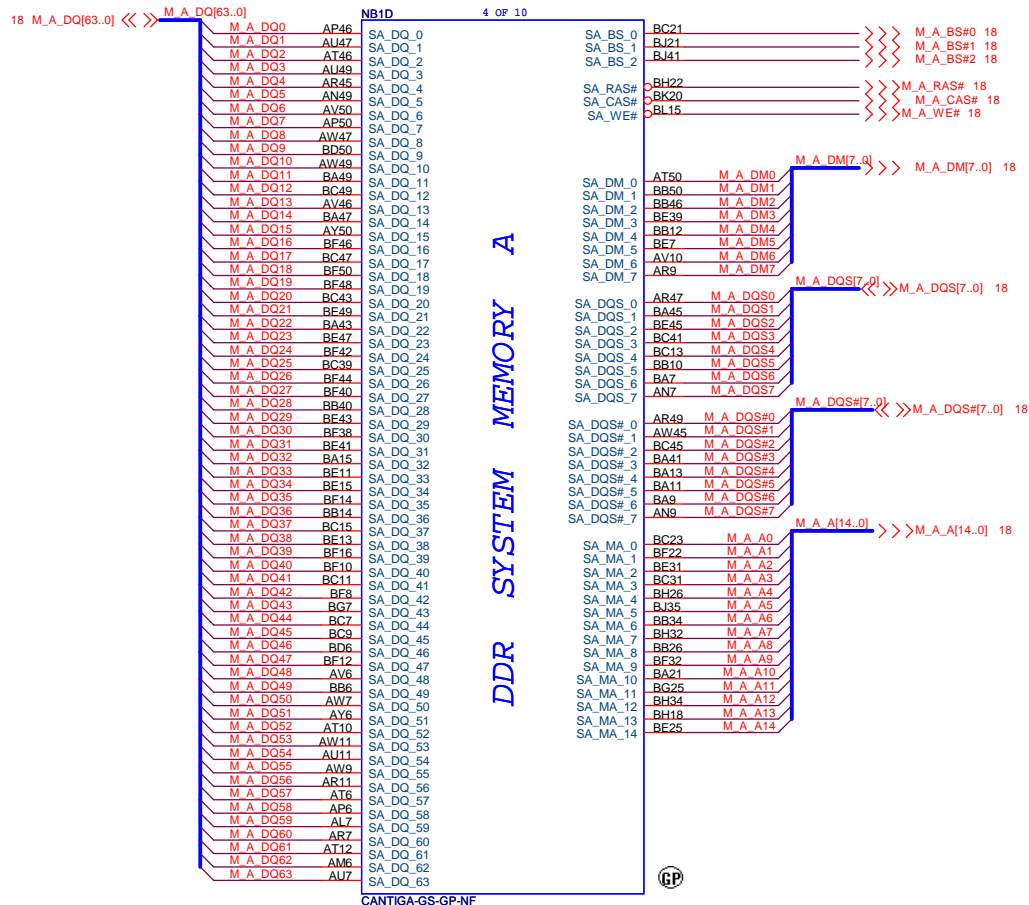
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

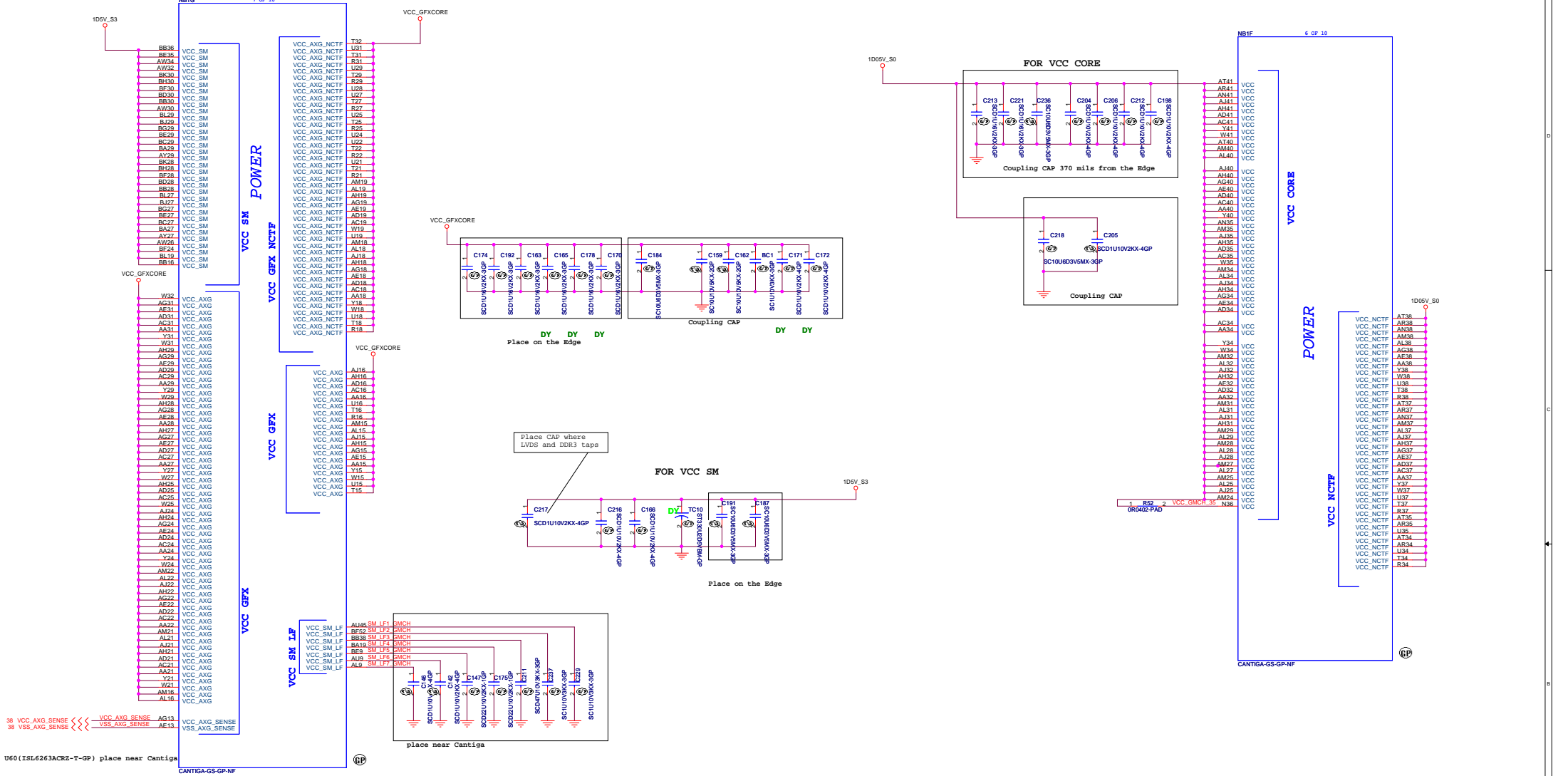
Title
Size Document Number
Date: Monday, April 06, 2009
Cantiga (1 of 6)
JM41 Discrete
Rev
-1
Sheet 7 of 48



FOR Cantiga: 1.02k_1 ohm
Teenah: 1.3k ohm
CRT IREF routing Trace
width use 20 mil

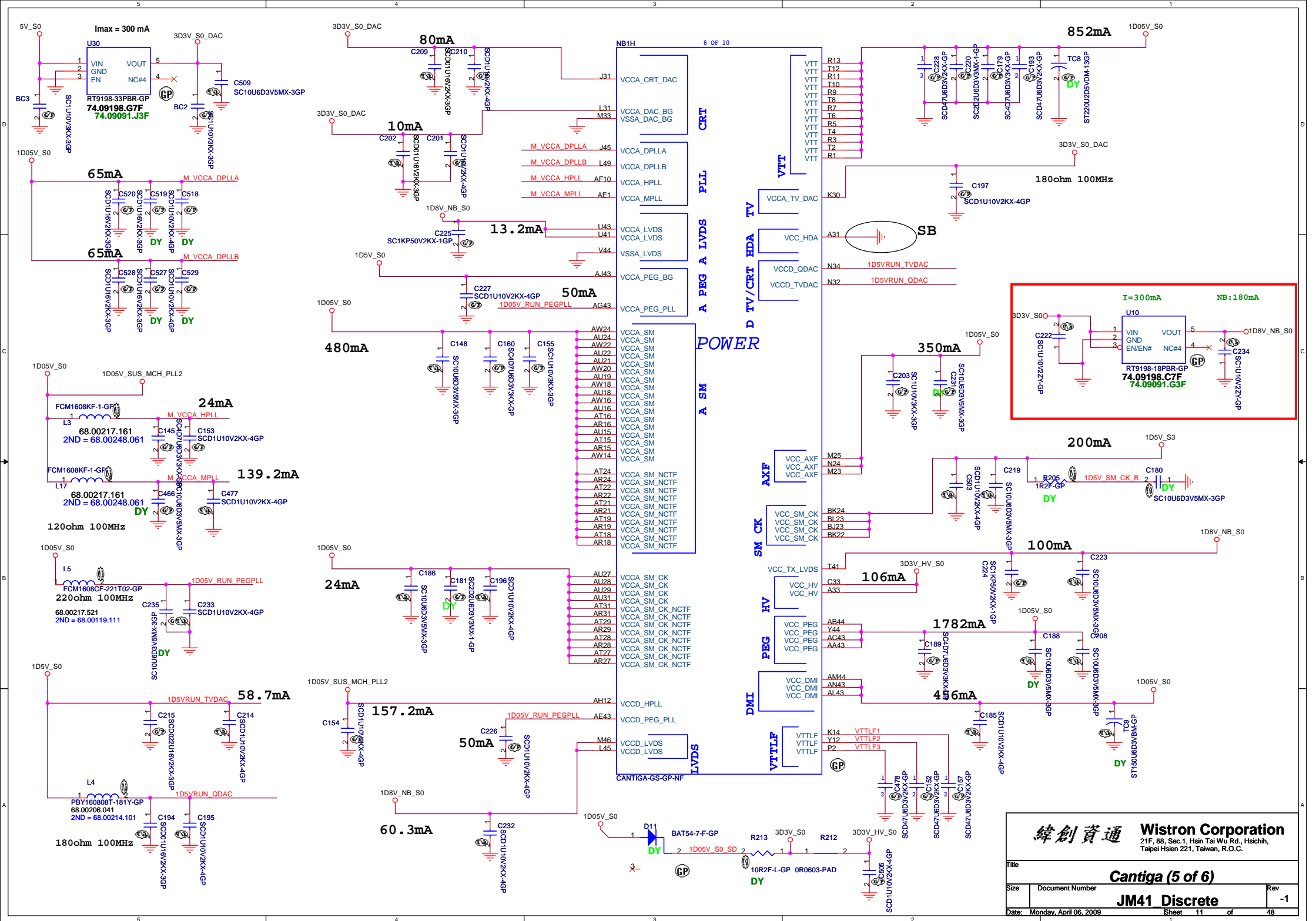


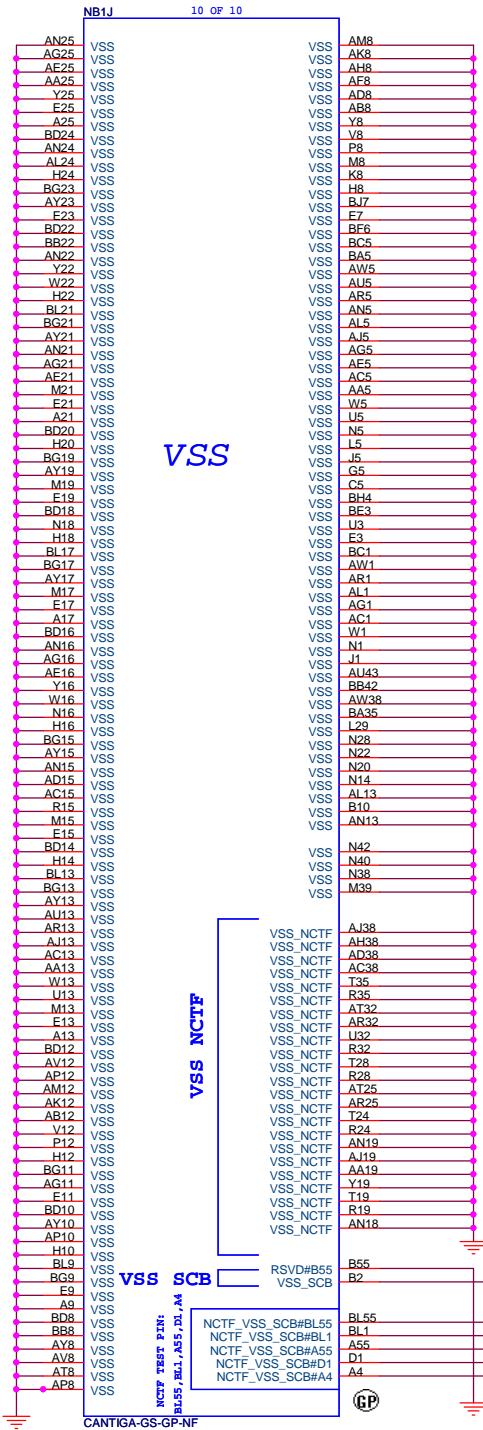
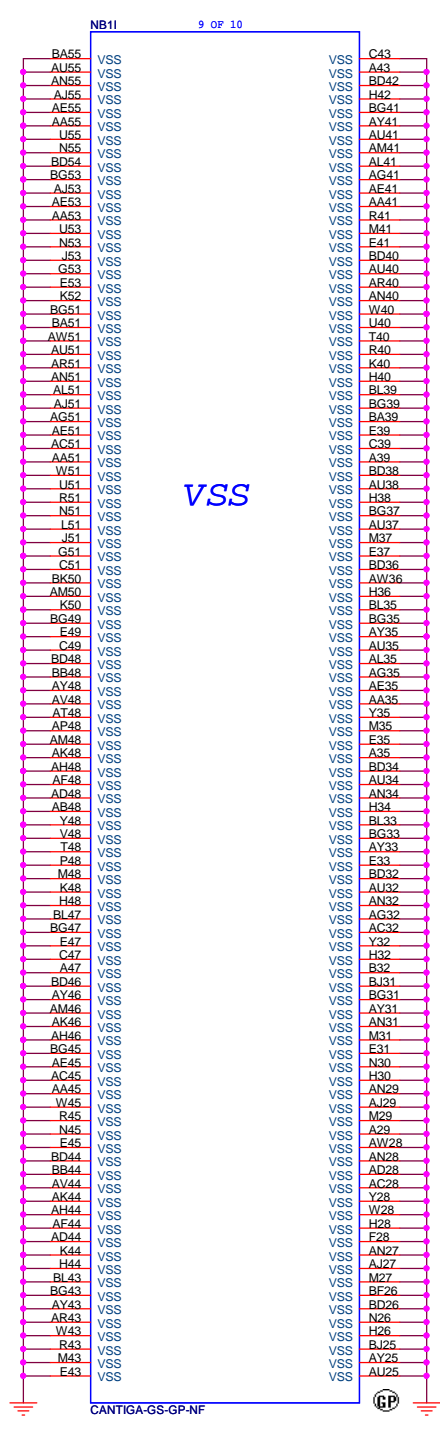




38 VCC_AKG_SENSE <<< VCC_AKG_SENSE AG13
38 VSS_AKG_SENSE <<< VSS_AKG_SENSE AE13

U60 (ISL6263ACRZ-T-OP) place near Cantiga

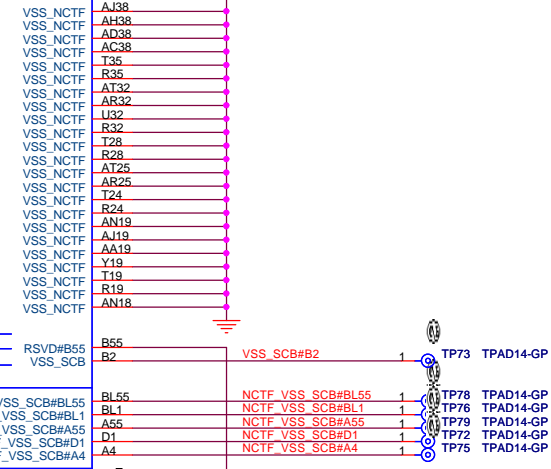




VSS

VSS NCTF

VSS SCB



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size Document Number

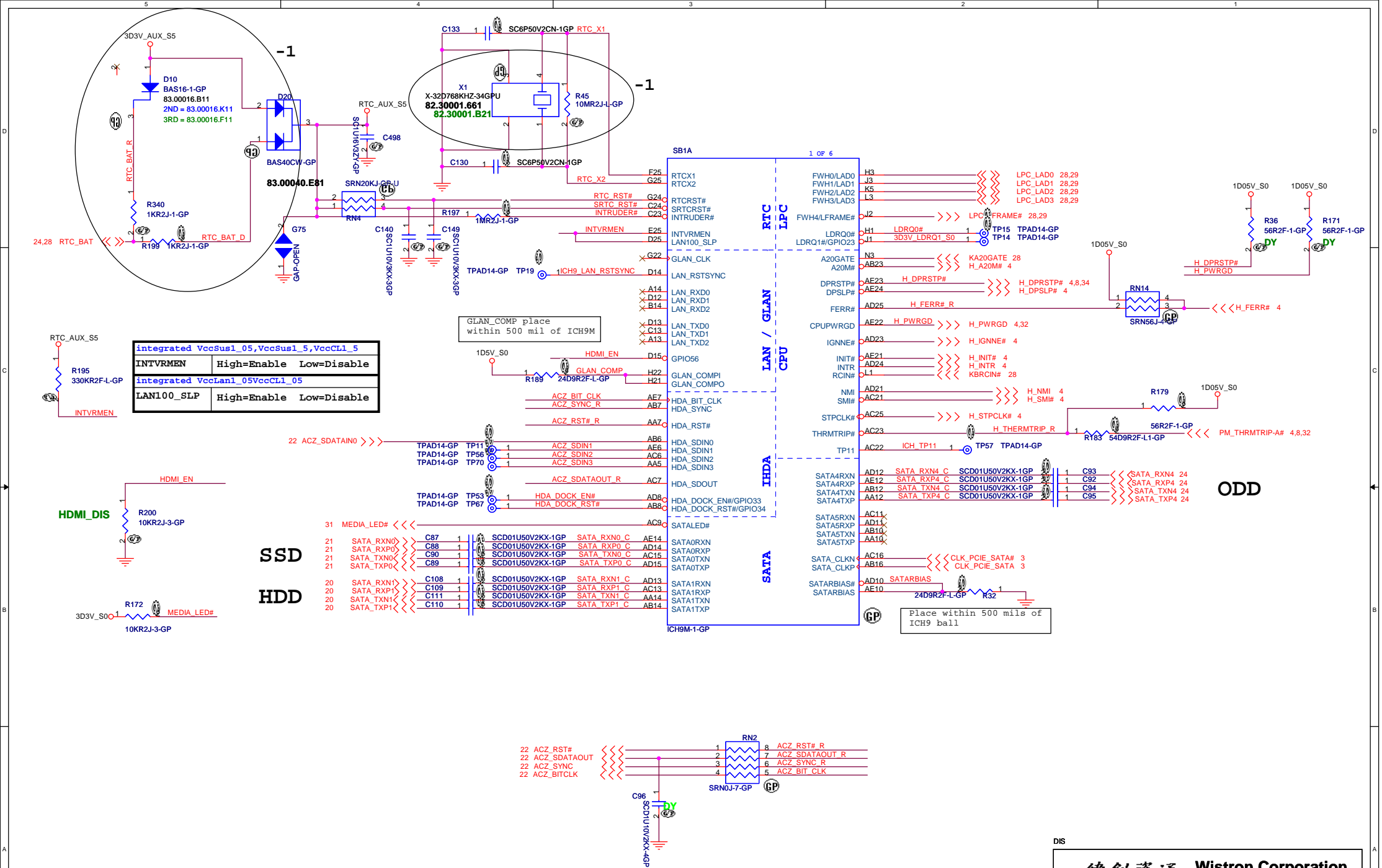
Date: Monday, April 06, 2009

Sheet 12 of 48

Rev -1

Cantiga (6 of 6)

JM41 Discrete



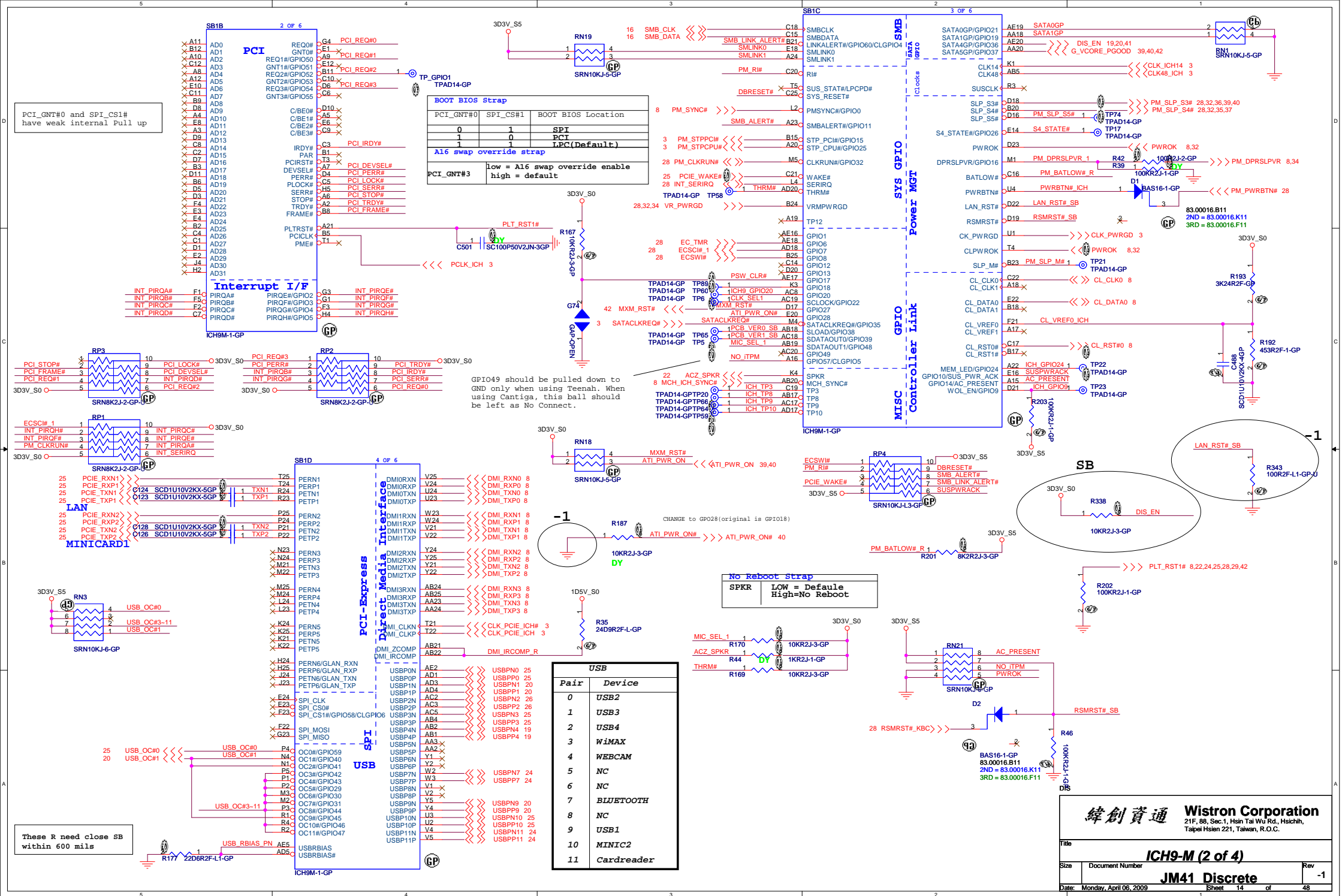
DIS

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (1 of 4)**

Size: Document Number: **JM41 Discrete** Rev: **-1**

Date: Monday, April 06, 2009 Sheet 13 of 48



657mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

2mA

2mA

47mA

SATA+USB=1.56A

USBPLL=10mA

19mA in S0; 78mA in S3/S4/S5

23mA

80mA

1mA

1.13A

23mA

50mA

1mA

VCC3_3=278mA

32mA

32mA

177mA

18mA

緯創資通

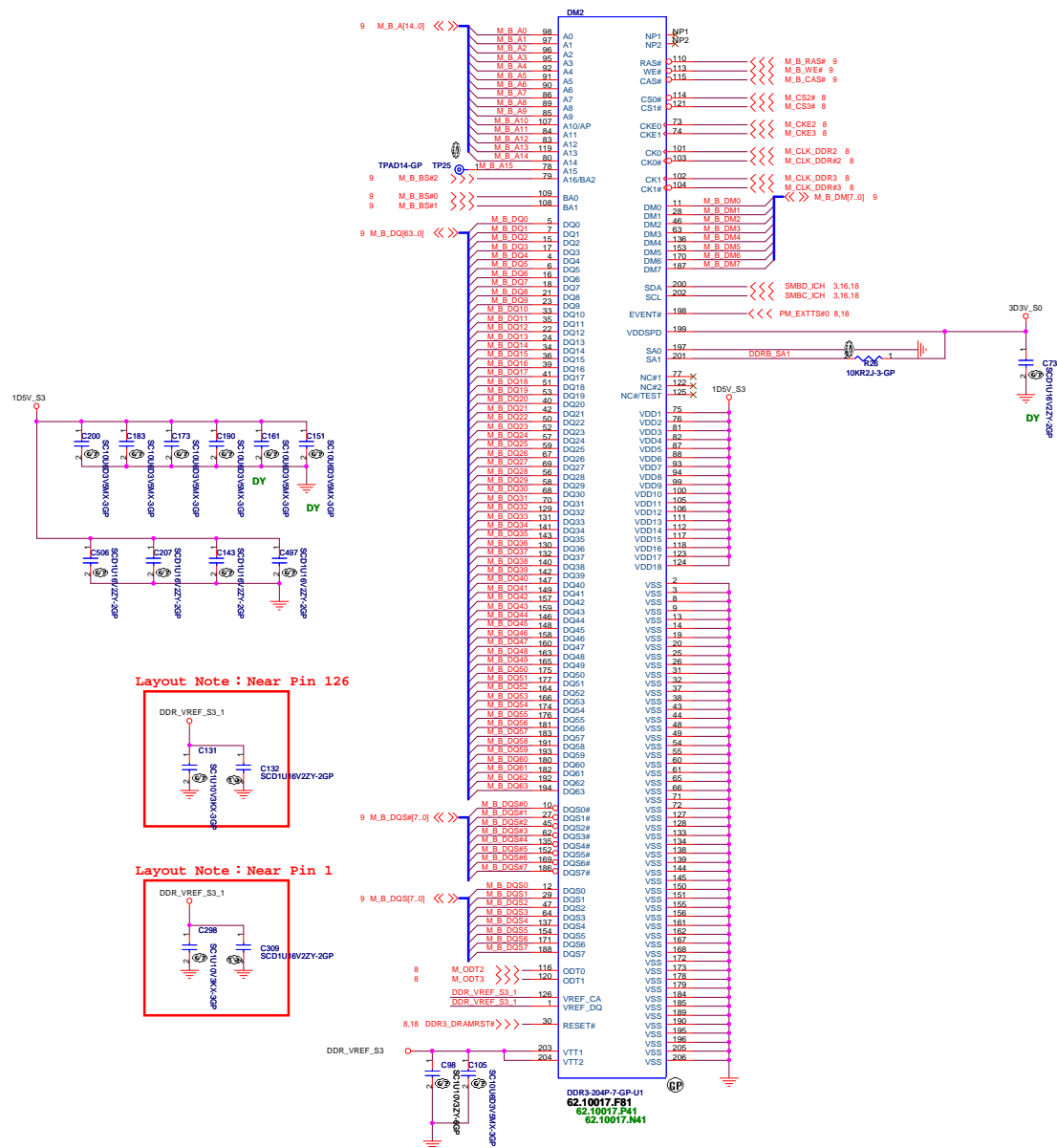
Wistron Corporation

21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

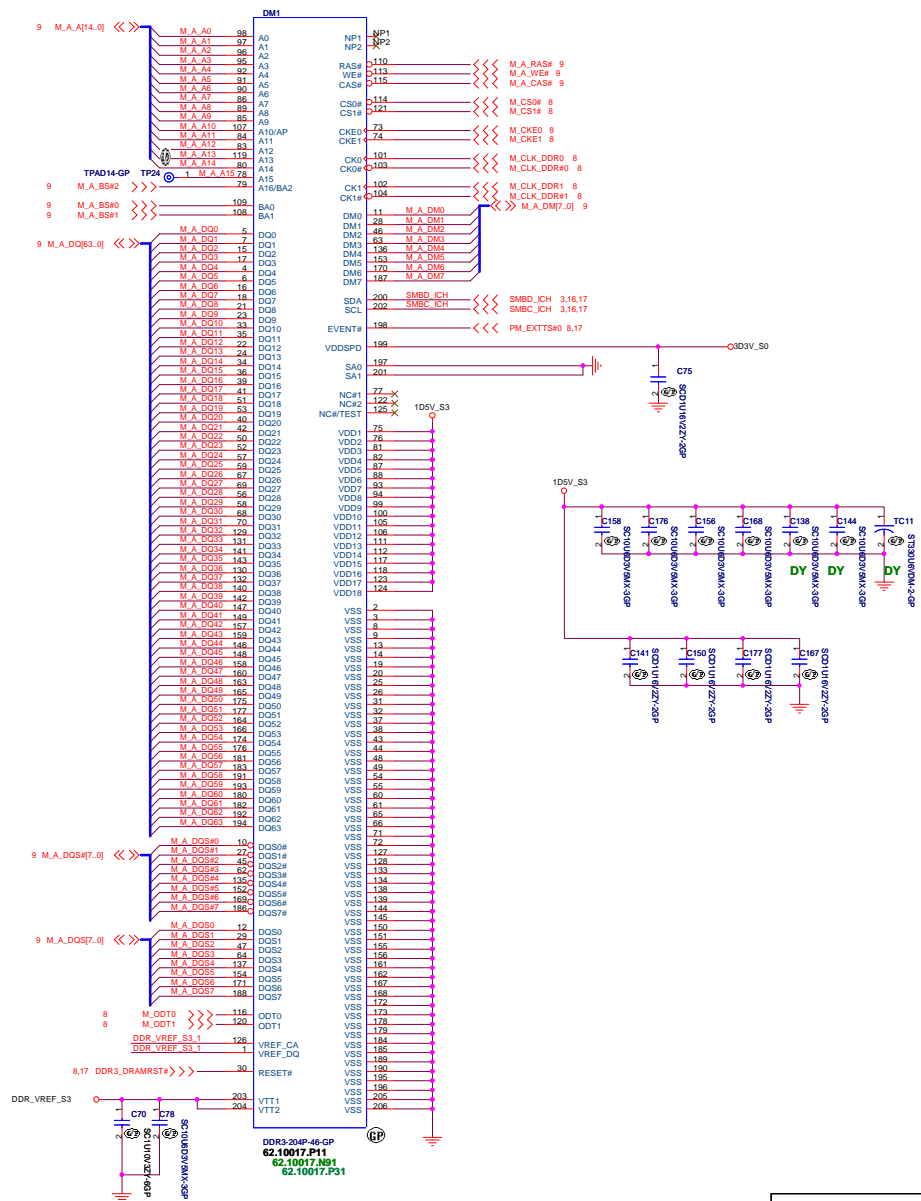
Title			ICH9-M (3 of 4)
Size	Document Number	Rev	
		JM41 Discrete	
Date:	Monday, April 06, 2009	Sheet	15 of 48



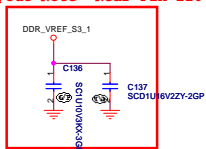
DDR3 SOCKET_1



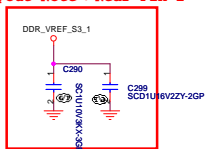
DDR3 SOCKET_2



Layout Note : Near Pin 126

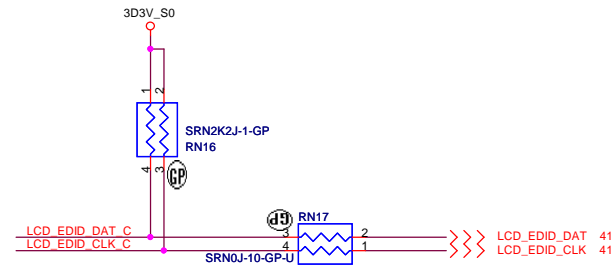
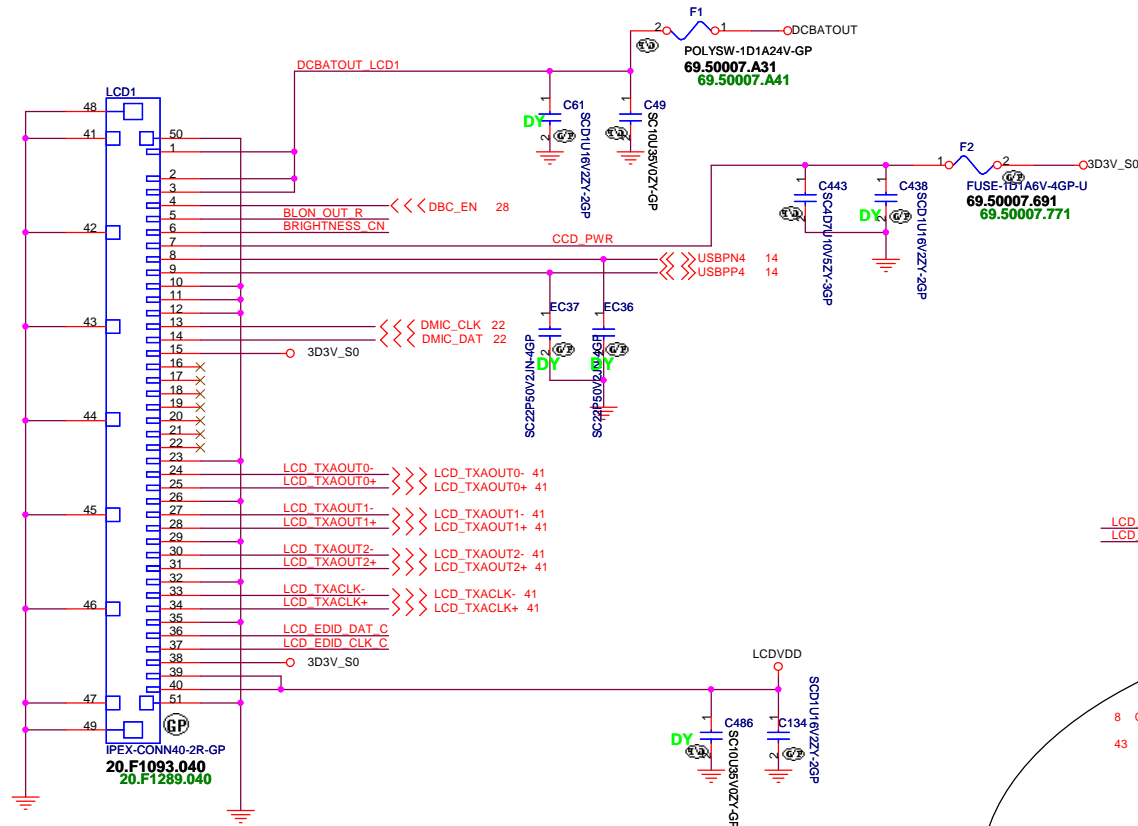


Layout Note : Near Pin 1

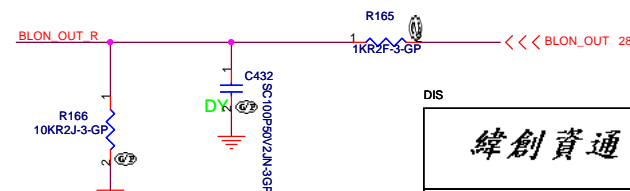
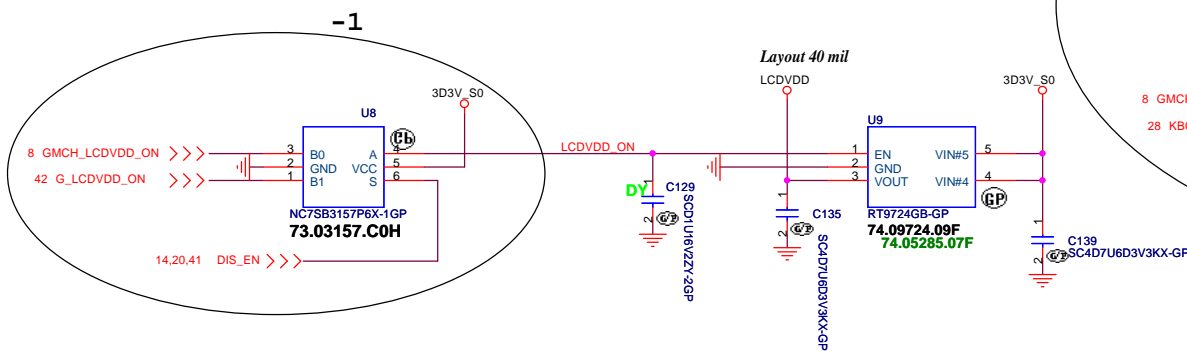
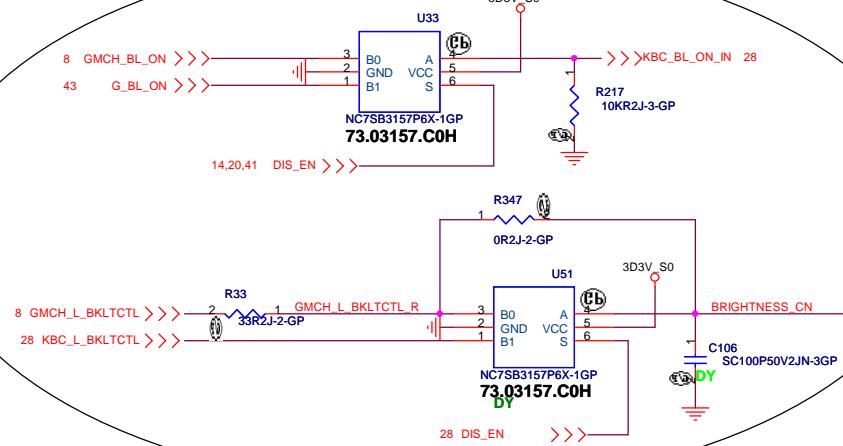


LCD/CCD CONN

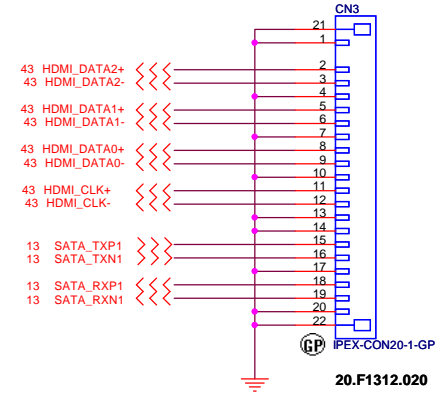
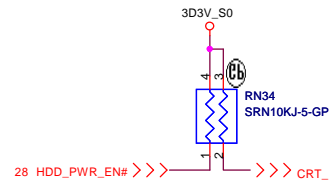
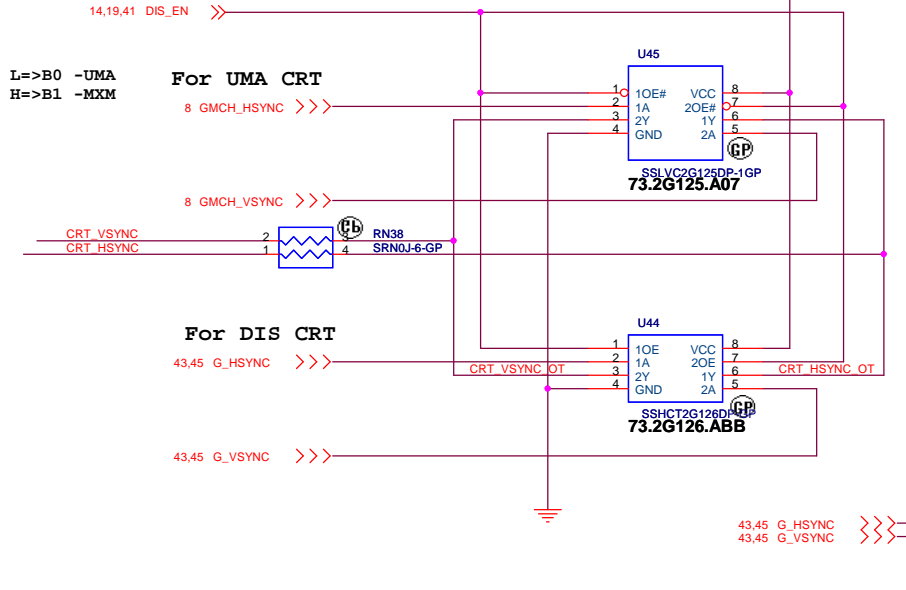
Internal MIC



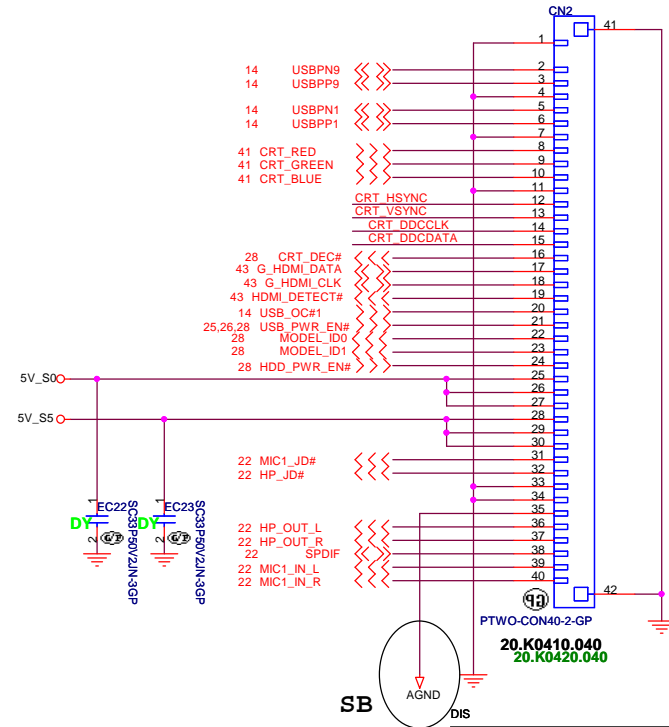
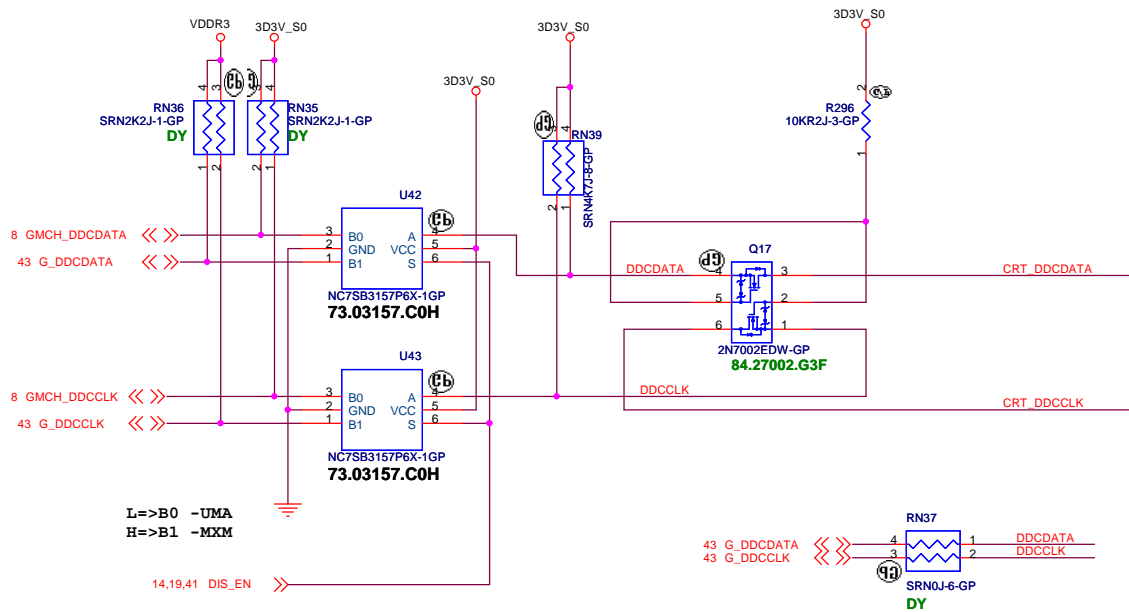
-1



Hsync & Vsync level shift

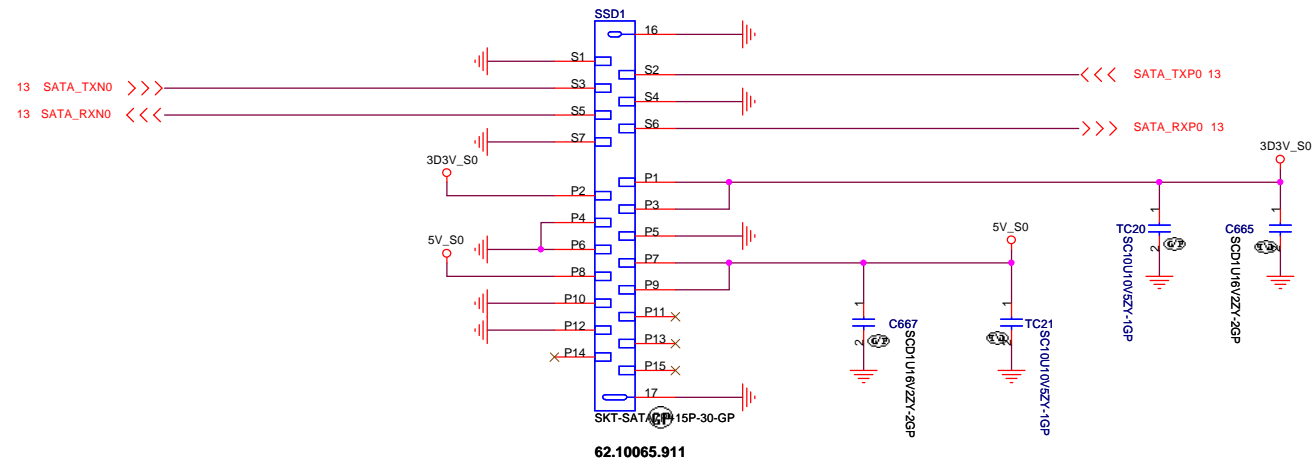


DDC_CLK & DATA level shift



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSD SATA Connector

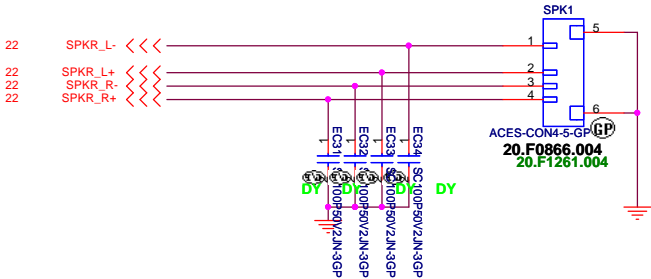


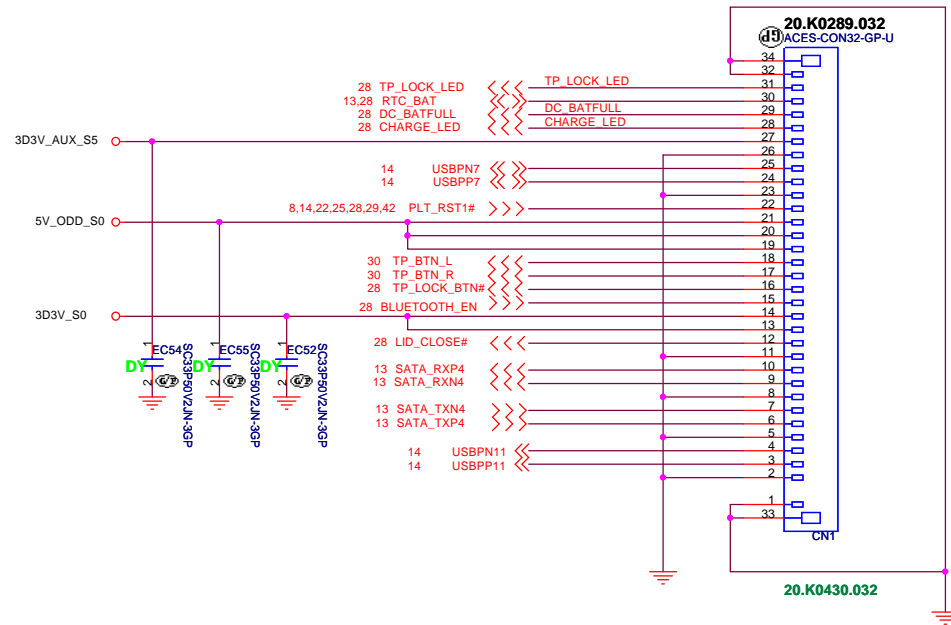
DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD CONN			
Size	Document Number	Rev	
	JM41 Discrete		-1
Date:	Monday, April 06, 2009	Sheet	21 of 48

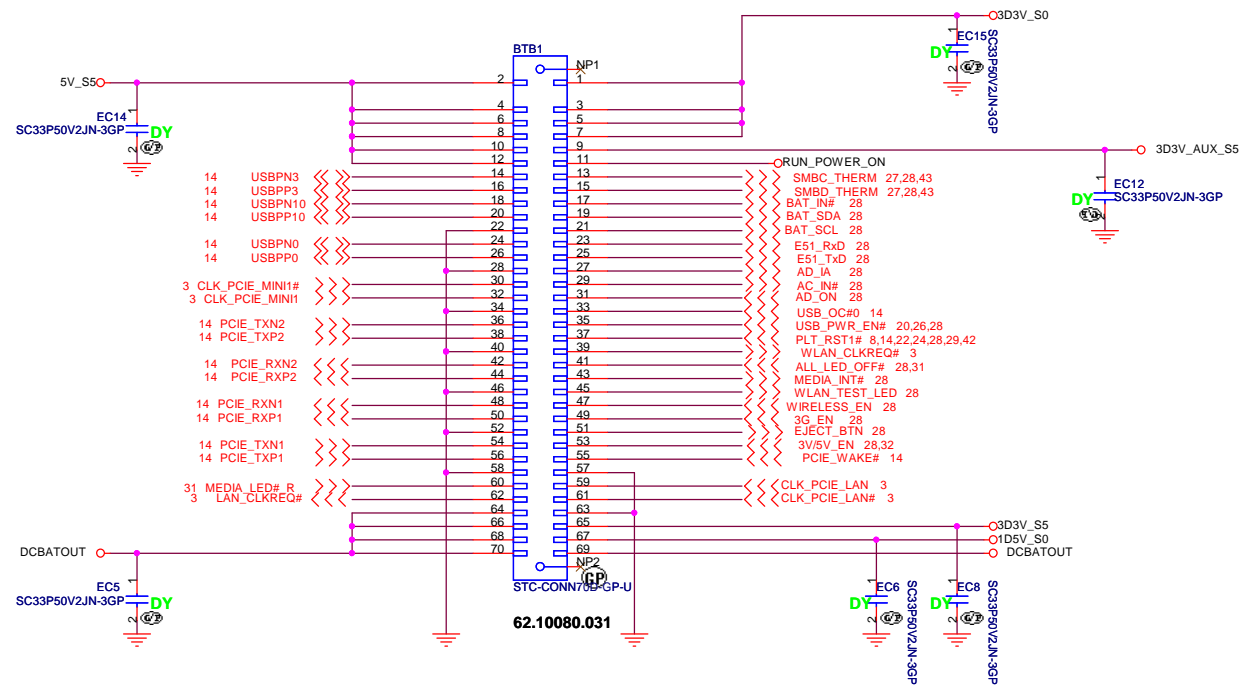
Internal Speaker





DIS

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CARDREADER BD CONN			
Size	Document Number		Rev
	JM41 Discrete		-1
Date:	Thursday, April 09, 2009	Sheet	24 of 48



DIS

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI BD CONN

Size
A3

Document Number

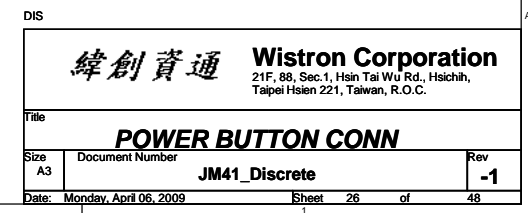
JM41_Discrete

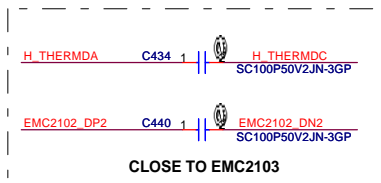
Rev

-1

Date: Monday, April 06, 2009

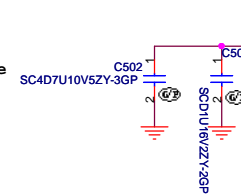
Sheet 25 of 48



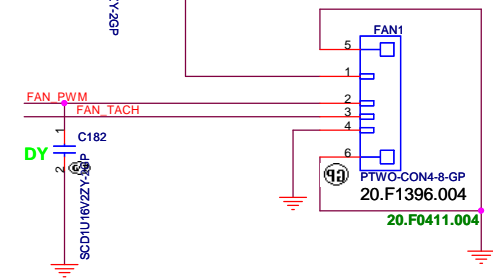
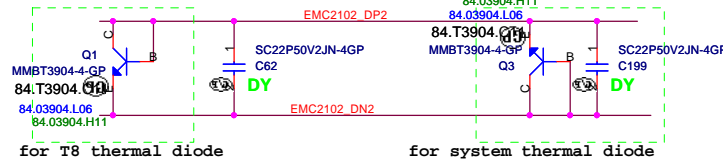
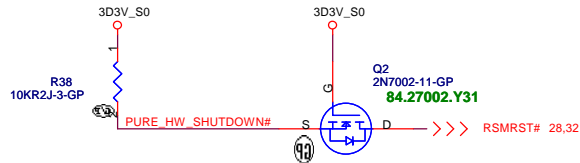


CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

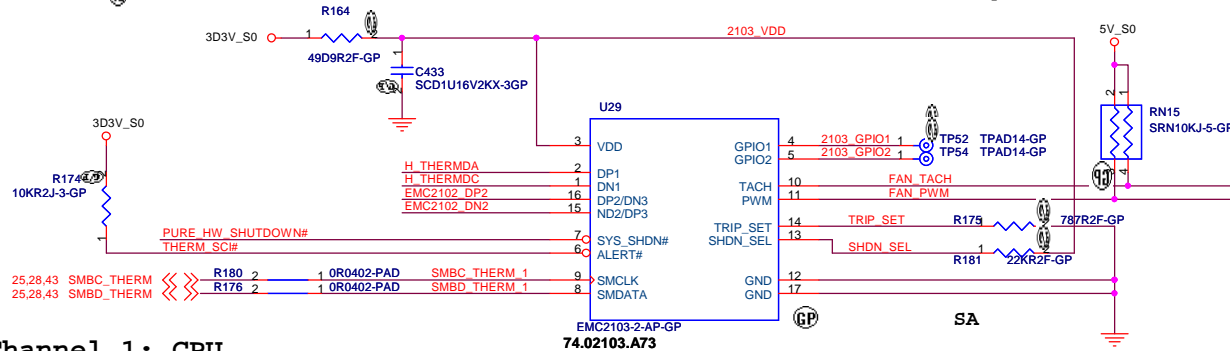
for CPU thermal diode



C587 for EMI and solve acoustic noise



ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL



Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN SEL

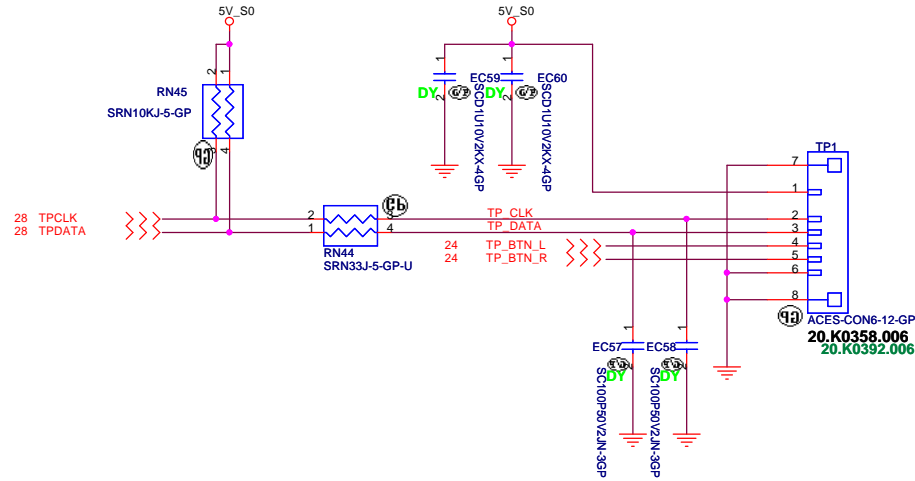
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

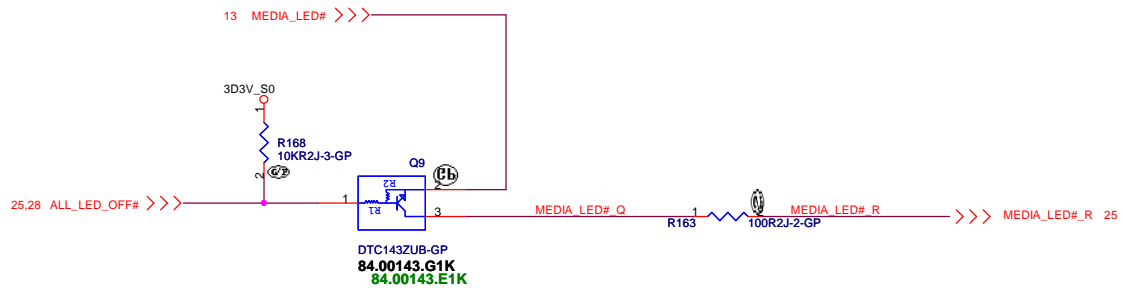
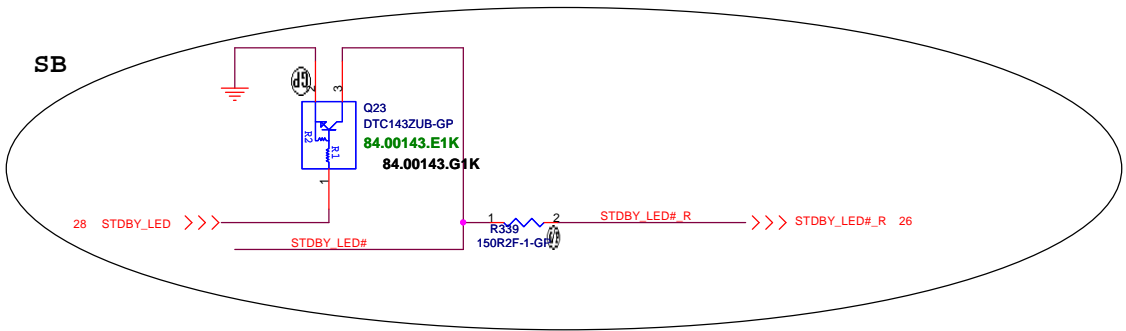
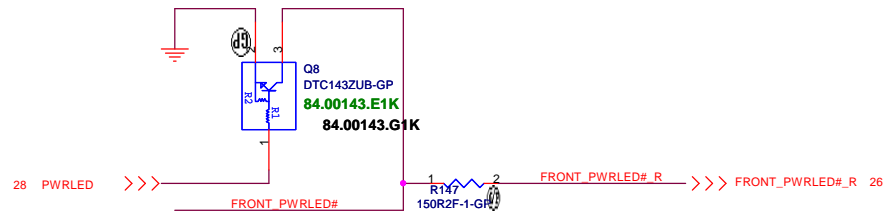
DIS

TOUCH PAD



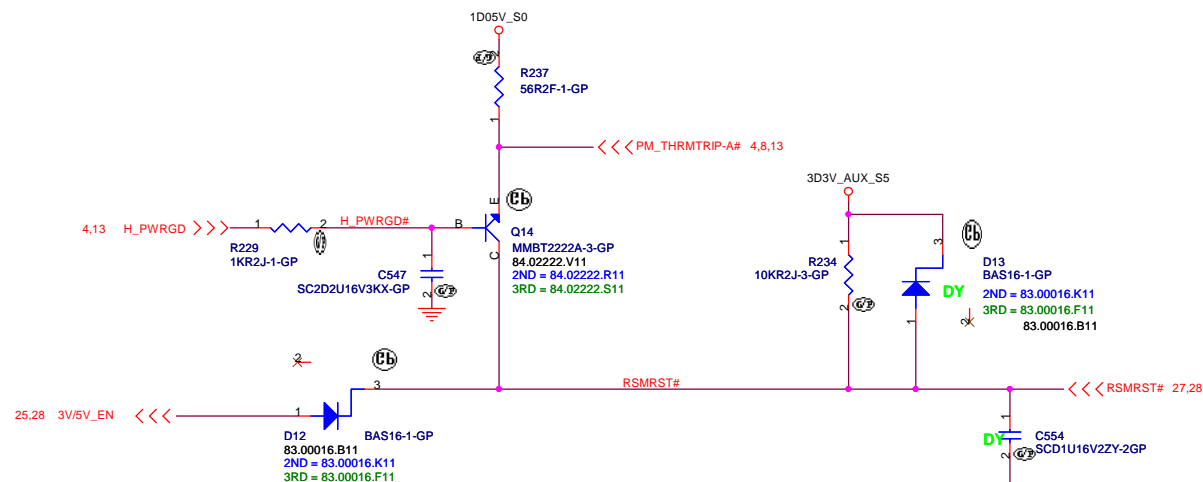
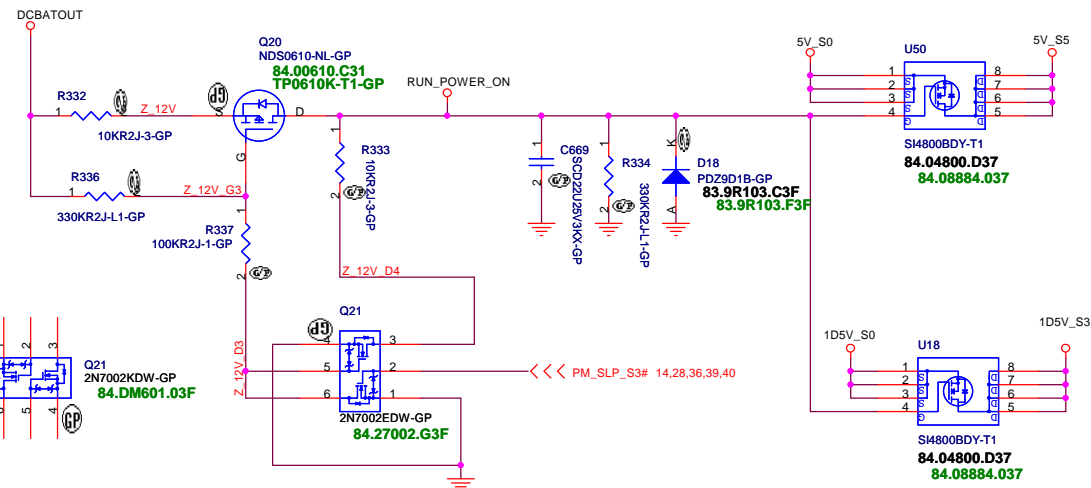
DIS

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Touch PAD			
Size	Document Number		Rev
	JM41 Discrete		-1
Date: Thursday, April 09, 2009		Sheet 30 of 48	

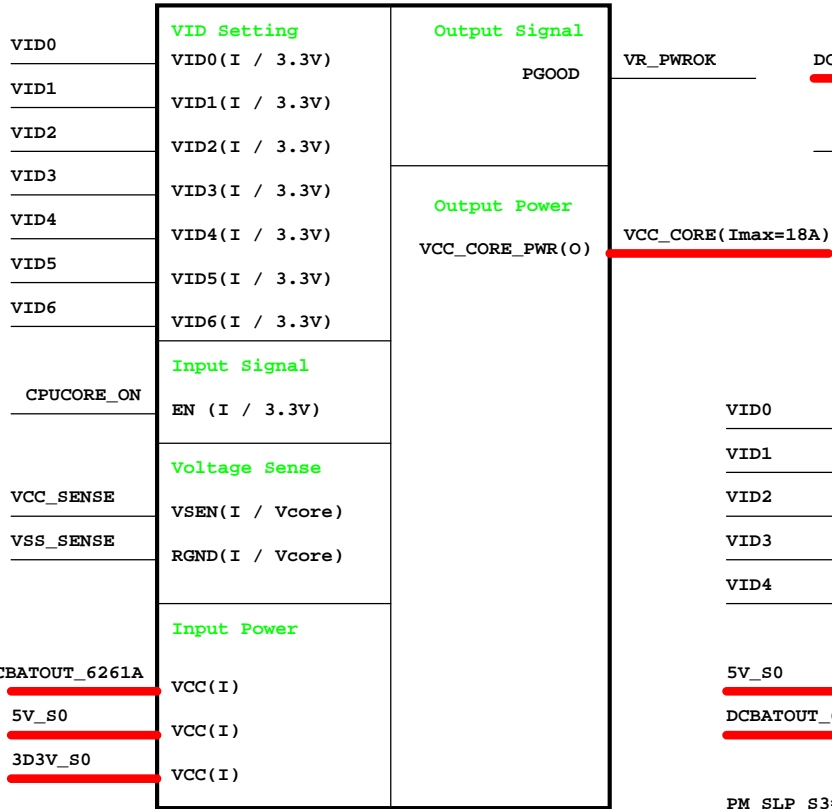


DIS

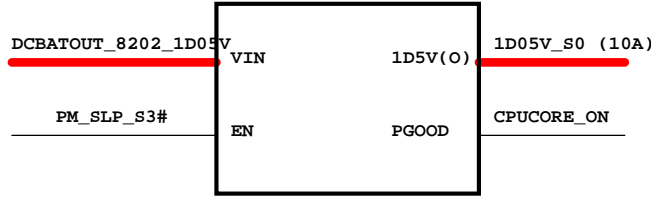
Run Power



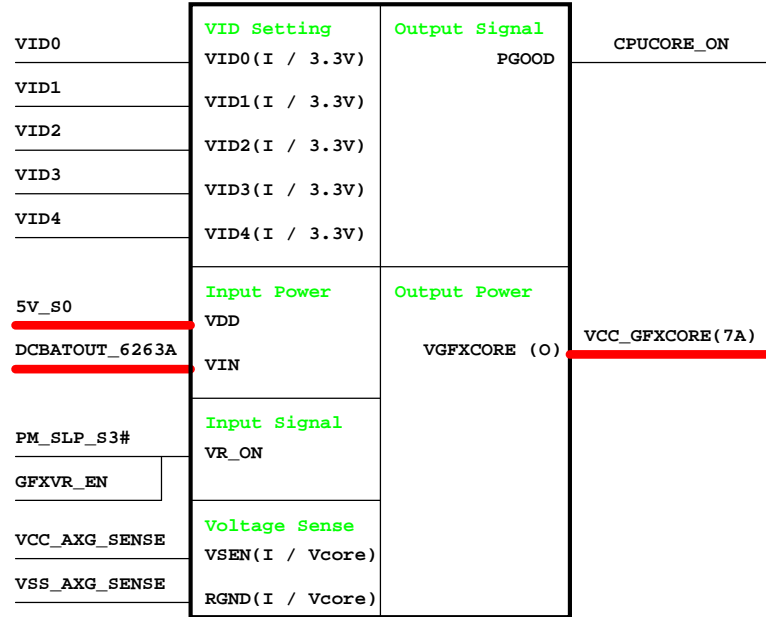
CPU_CORE
ISL6261A



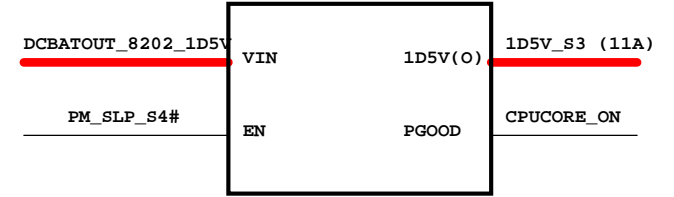
RT8202 1D05V_S0



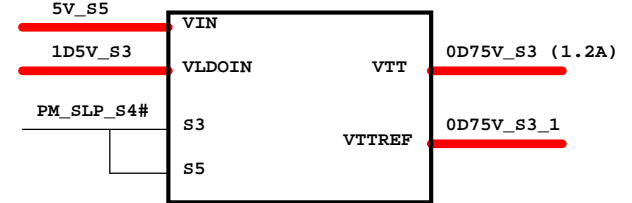
GFX_CORE
ISL6263A



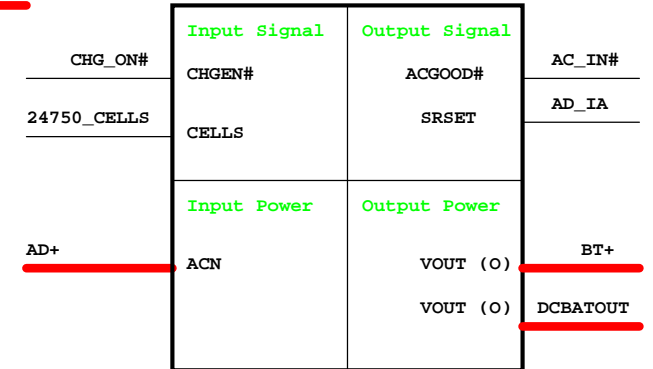
RT8202 1D5V_S3



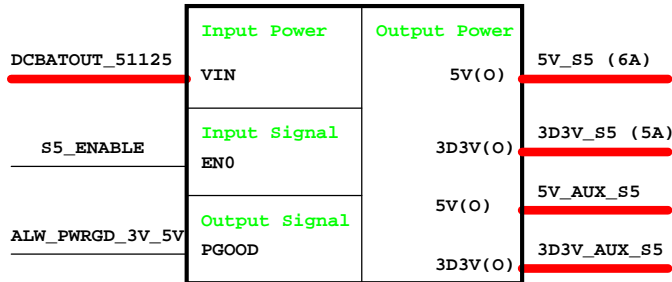
RT9026 0D9V_S0



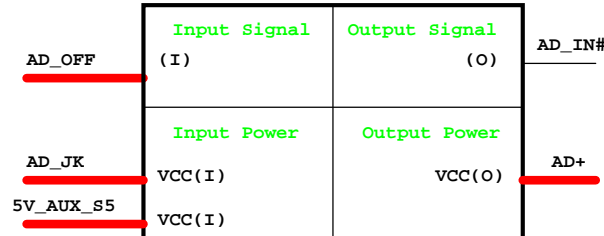
Charger MAX8731A



TPS51125
5V/3D3V

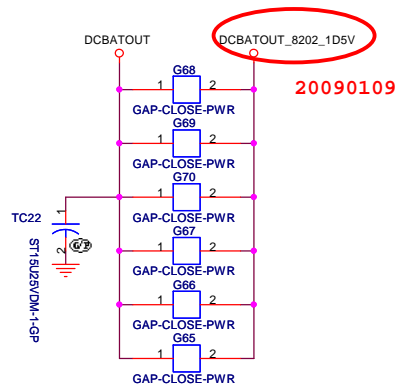


Adapter



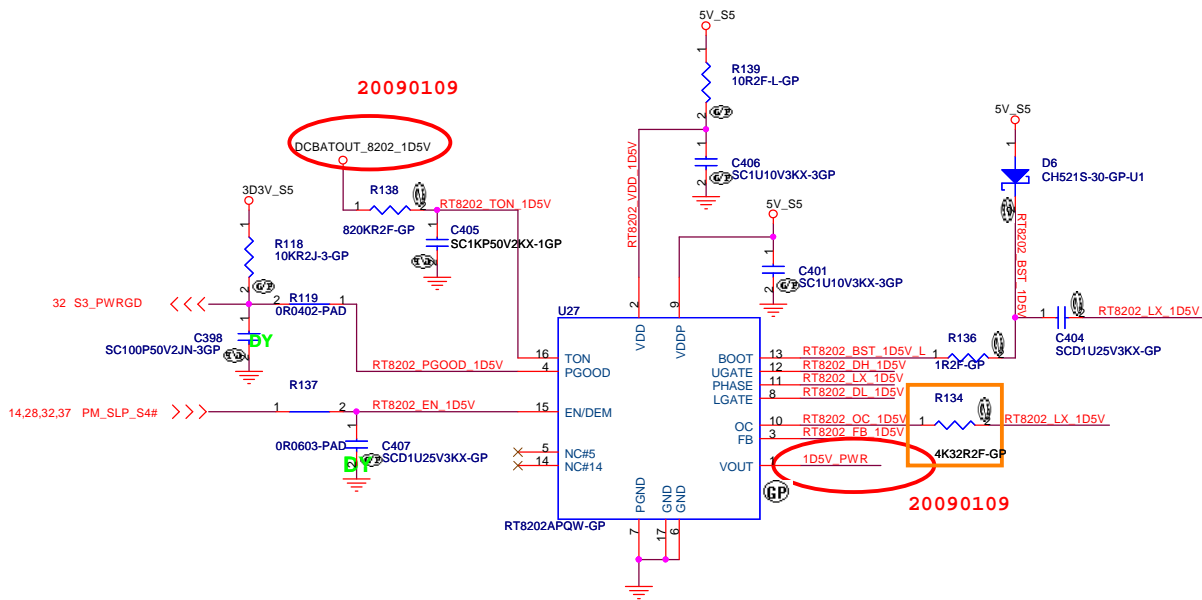
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Power Sequence Logic			
Size B	Document Number	JM41 Discrete	Rev -1
Date: Monday, April 06, 2009	Sheet 33	of 48	

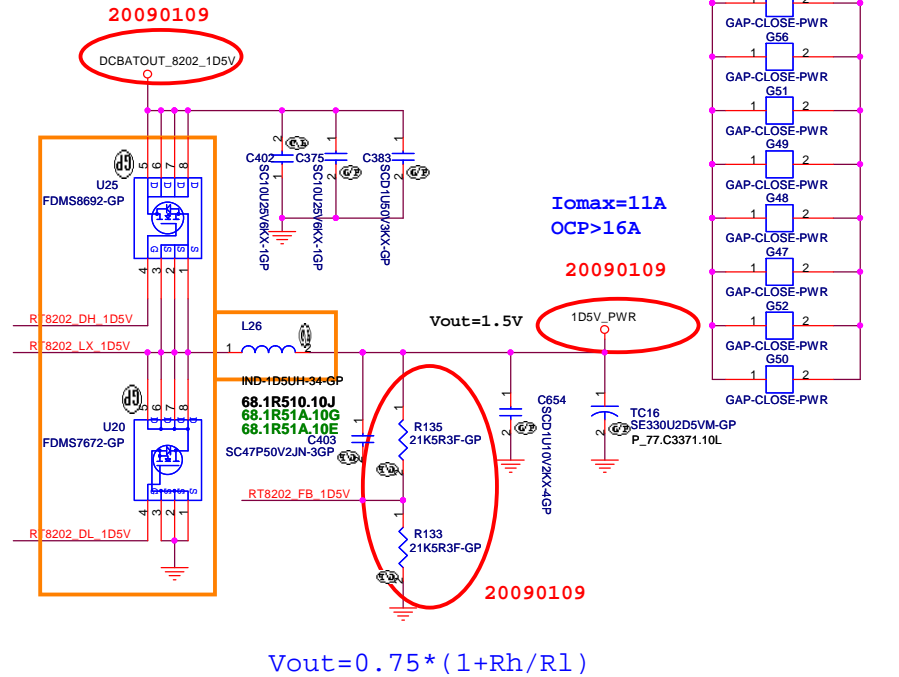


20090109

20090109



20090109



$I_{omax}=11A$
 $OCP>16A$

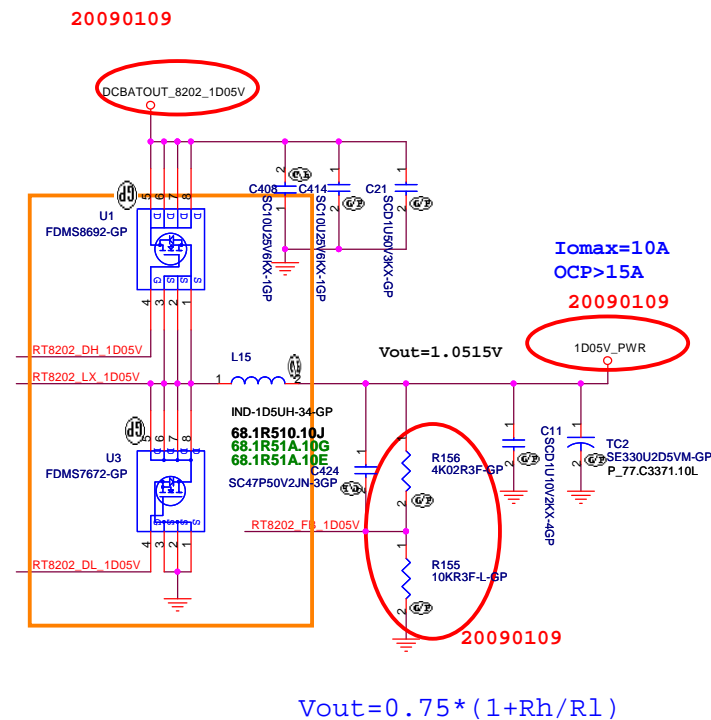
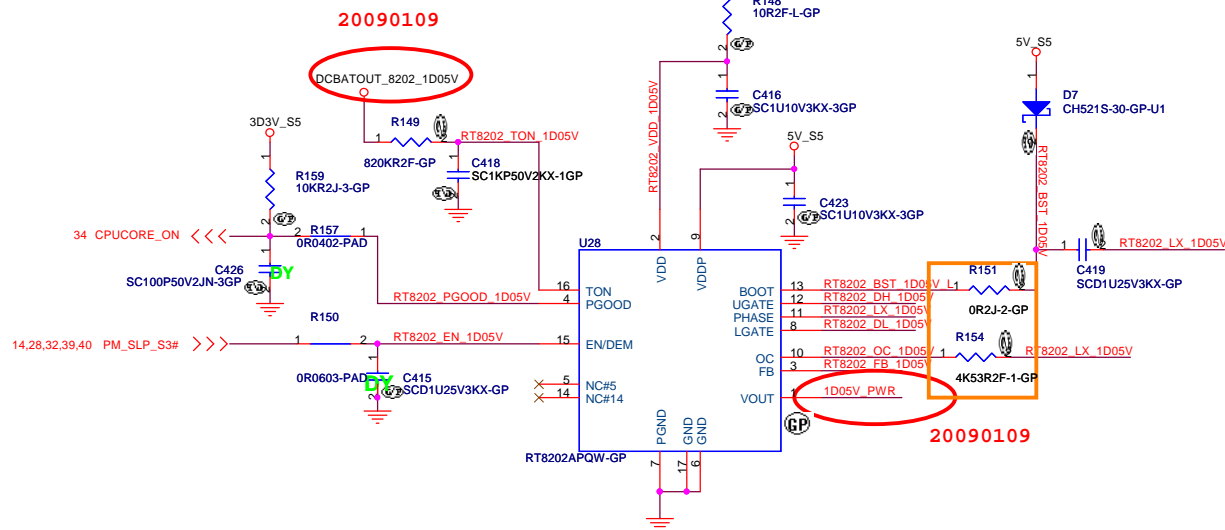
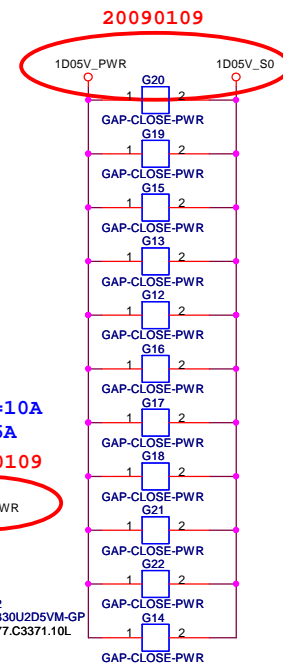
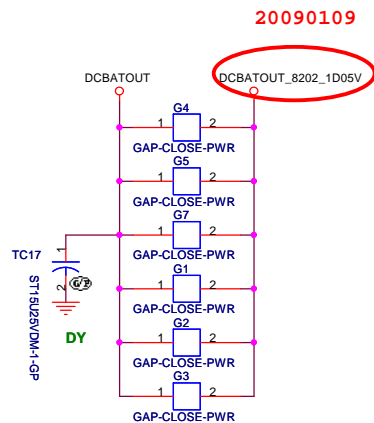
20090109

$V_{out}=0.75*(1+R_h/R_l)$

DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

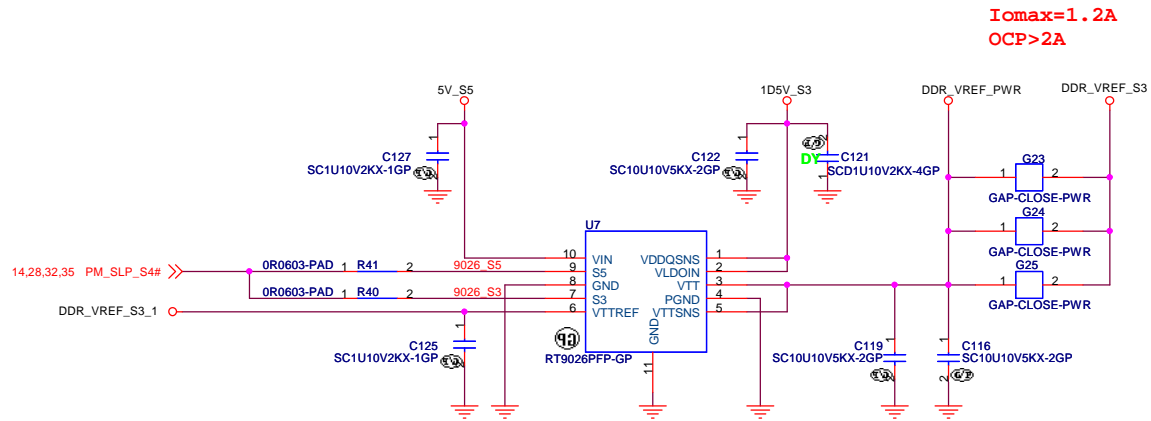
Title			RT8202 1D5V	
Size	Document Number	JM41 Discrete		Rev
A3				-1
Date:	Monday, April 13, 2009	Sheet	35	of 48



D15

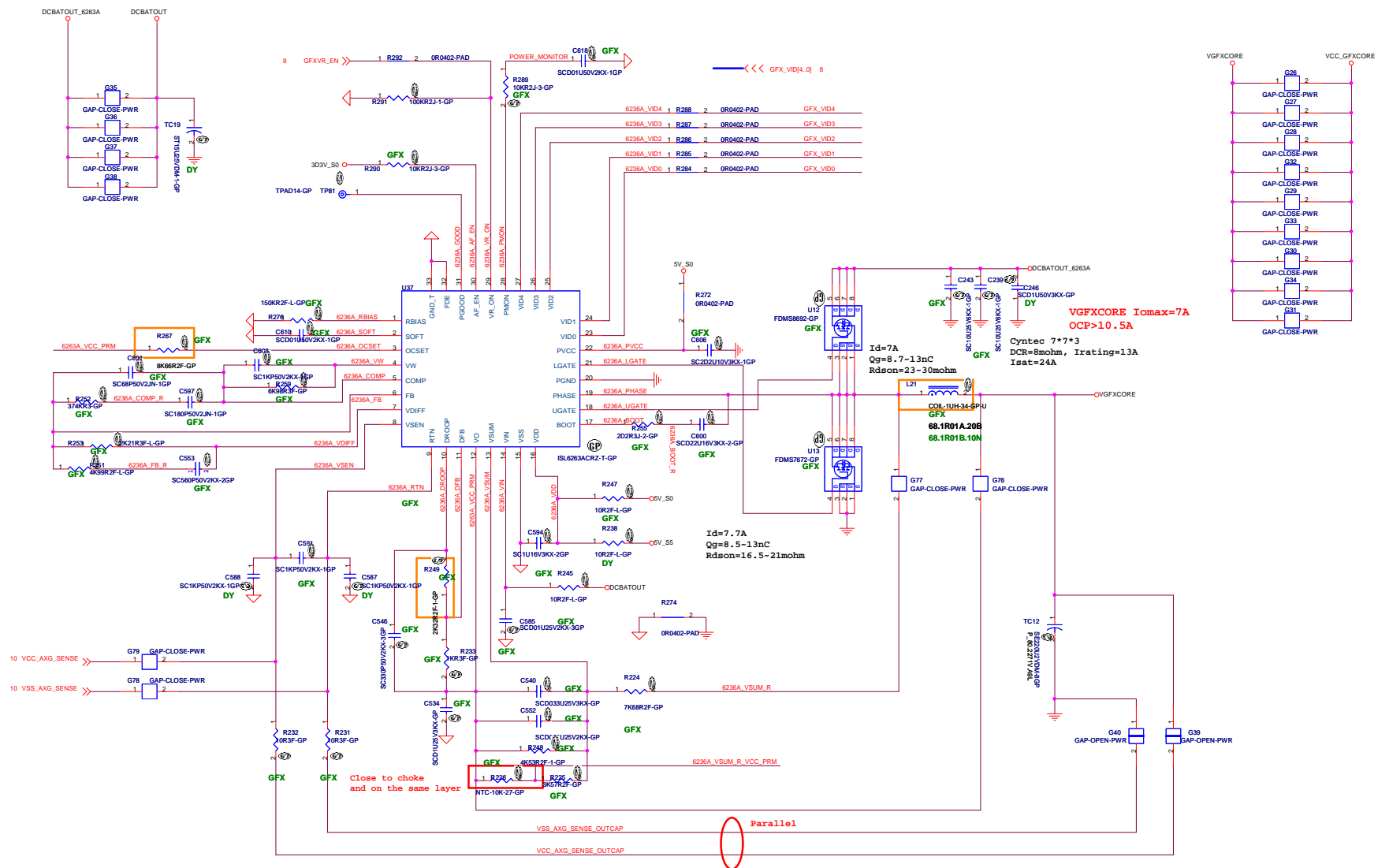
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

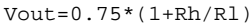
Title		
RT8202 1D05V		
Size	Document Number	Rev
A3	JM41 Discrete	-1
Date:	Monday, April 13, 2009	Sheet 36 of 48



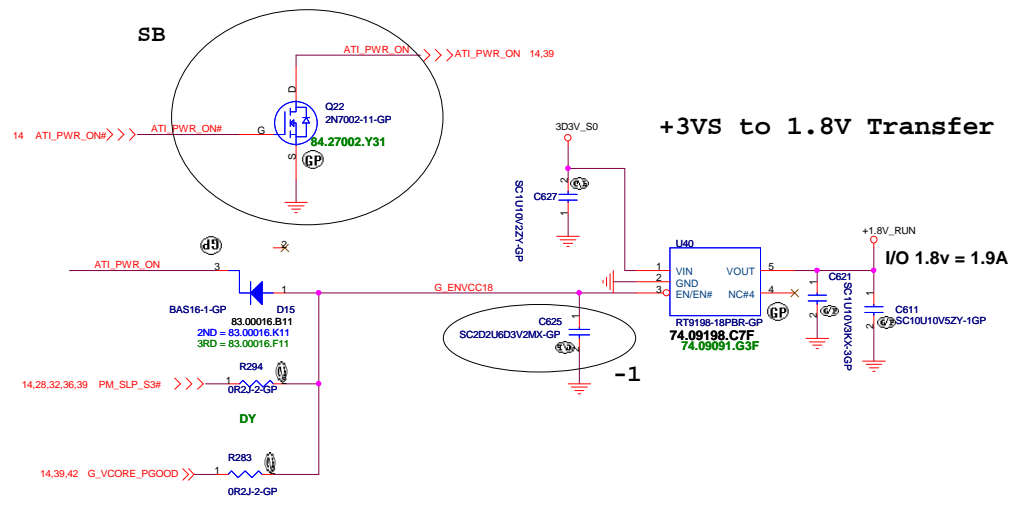
DIS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
RT9026 0D75V			
Size	Document Number	Rev	
A3	JM41 Discrete	-1	
Date:	Monday, April 06, 2009	Sheet	37 of 48

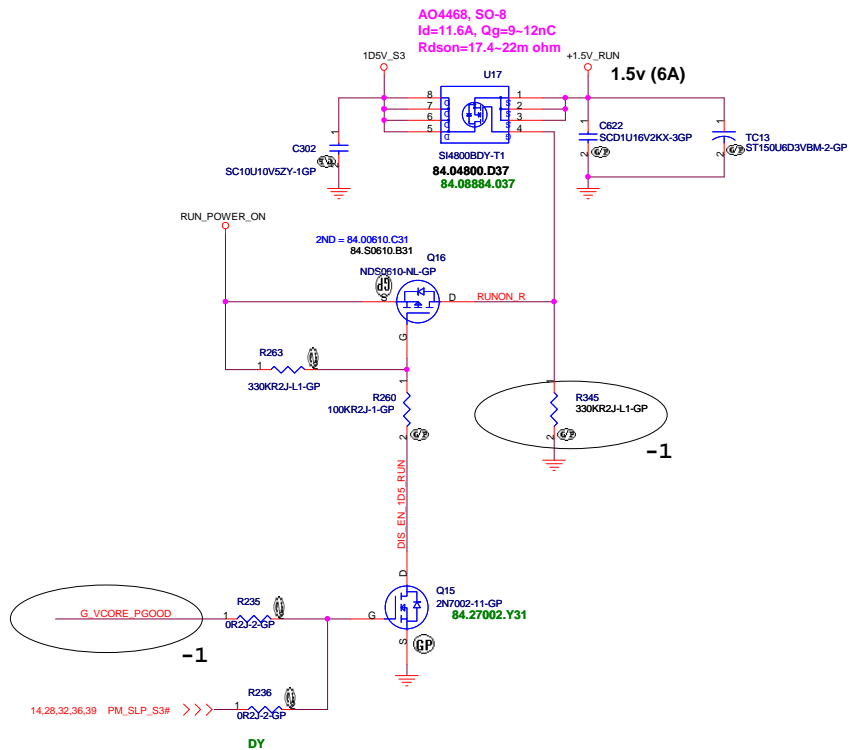




<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;">  <p>緯創資通</p> </div> <div> <p>Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p> </div> </div>			
Title			
RT8202A VGA CORE			
A3	Document Number		Rev
JM41 Discrete			-1
Date:	Monday, April 06, 2009		Sheet 39 of 48

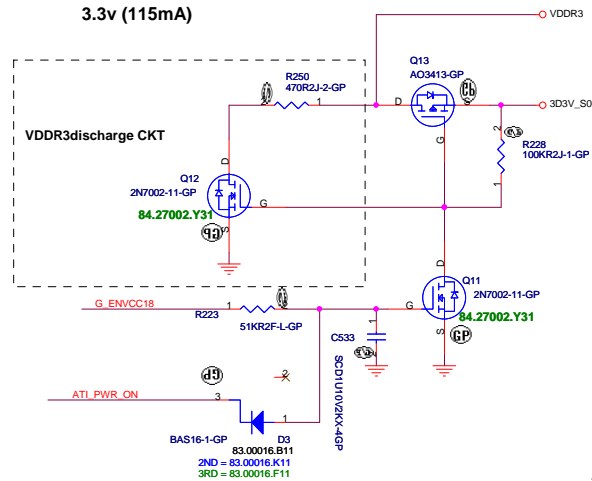


+1.5V to +1.5VS_RUN Transfer

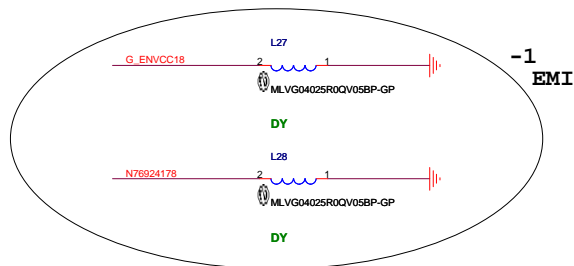
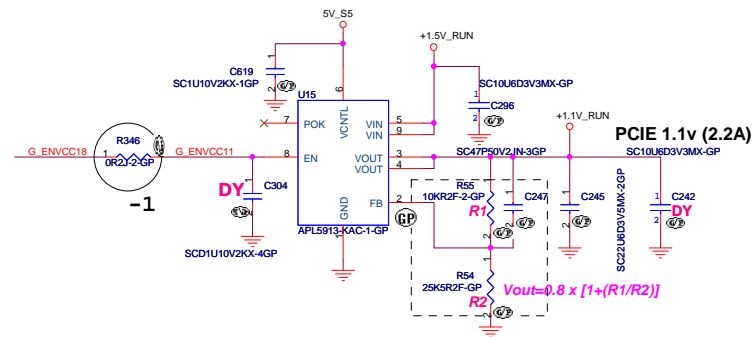


+3VS to 3.3V_DELAY Transfer

3.3v (115mA)

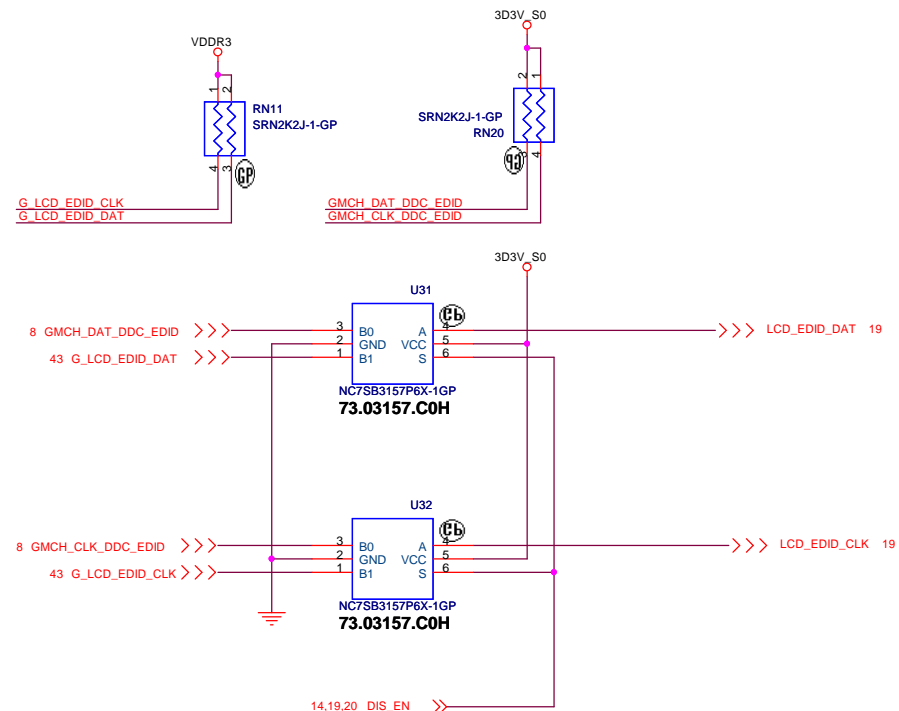


+1.5v to PCIE 1.1V Transfer



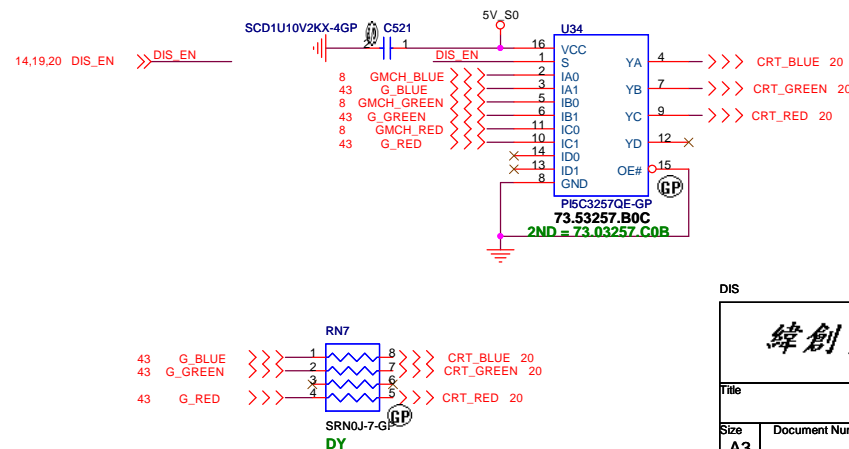
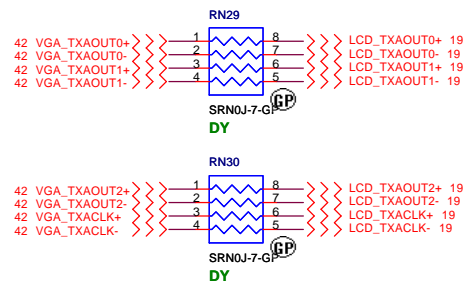
DIS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title			
M92S2 power			
Size	Document Number	Rev	
Custom	JM41 Discrete	-1	
Date:	Monday, April 13, 2009	Sheet	40 of 48



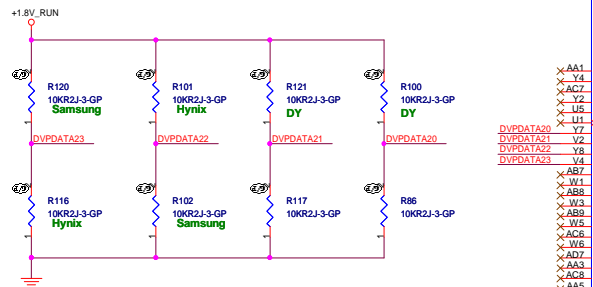
\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

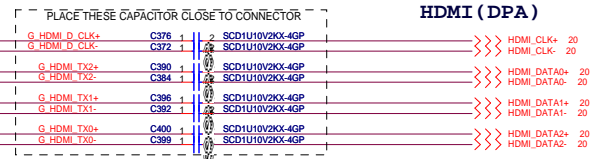
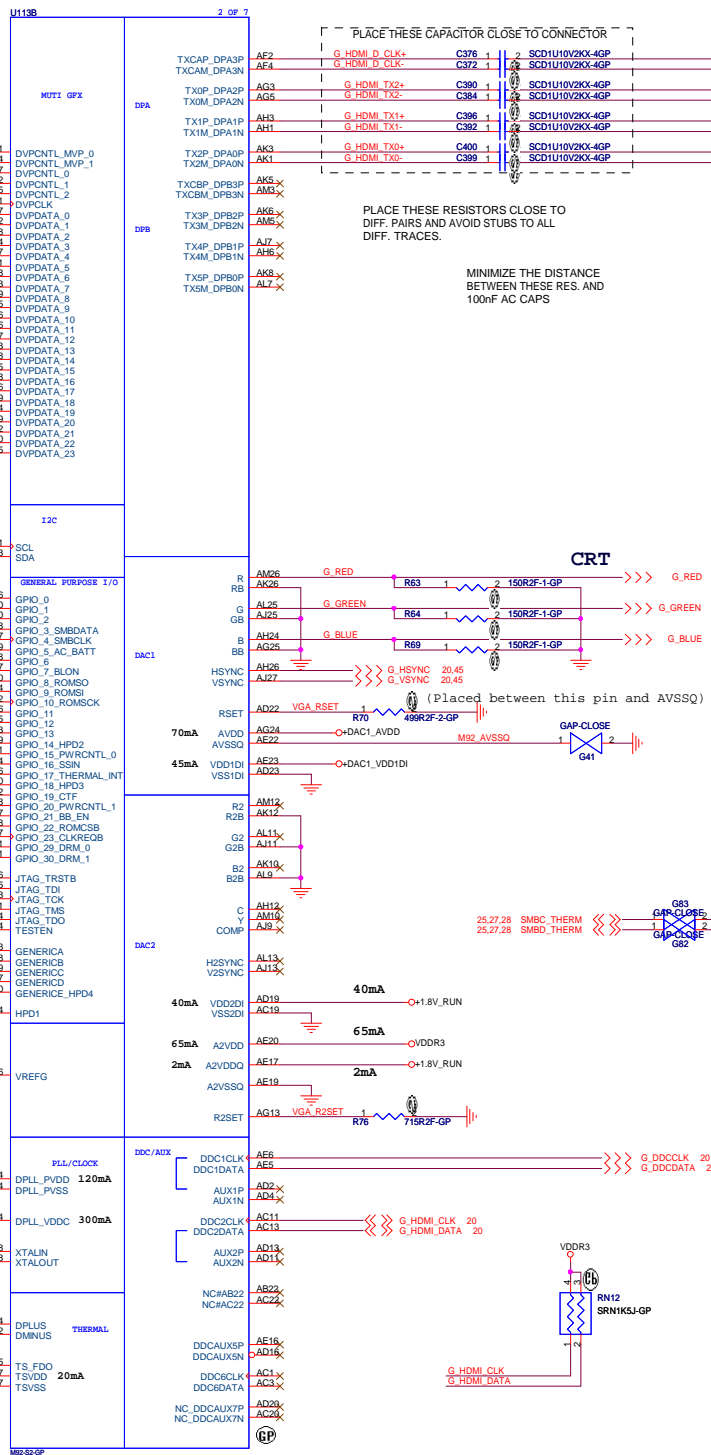
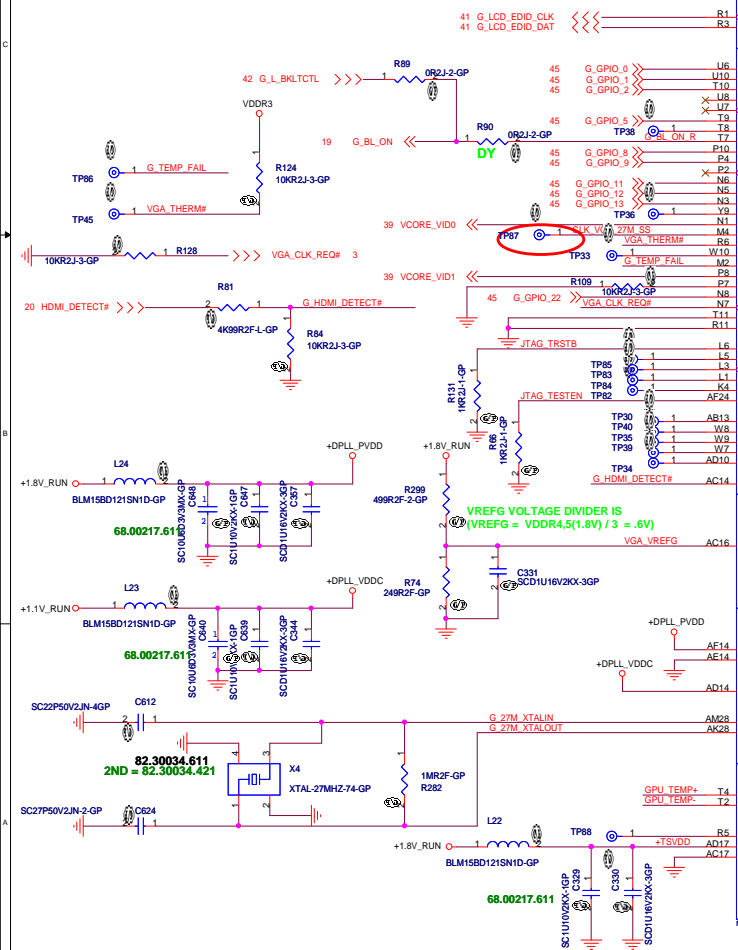


SSID = VIDEO

```
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
```

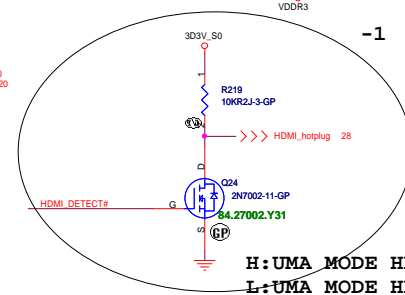
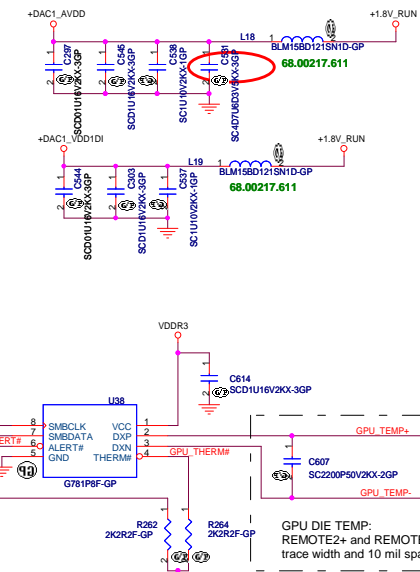


STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO
		0000 - GDDR3 16Mx32 Qimonda
		0001 - GDDR3 32Mx32 Hynix
		0010 - GDDR3 32Mx32 Qimonda
		0011 - GDDR3 32Mx32 Samsung



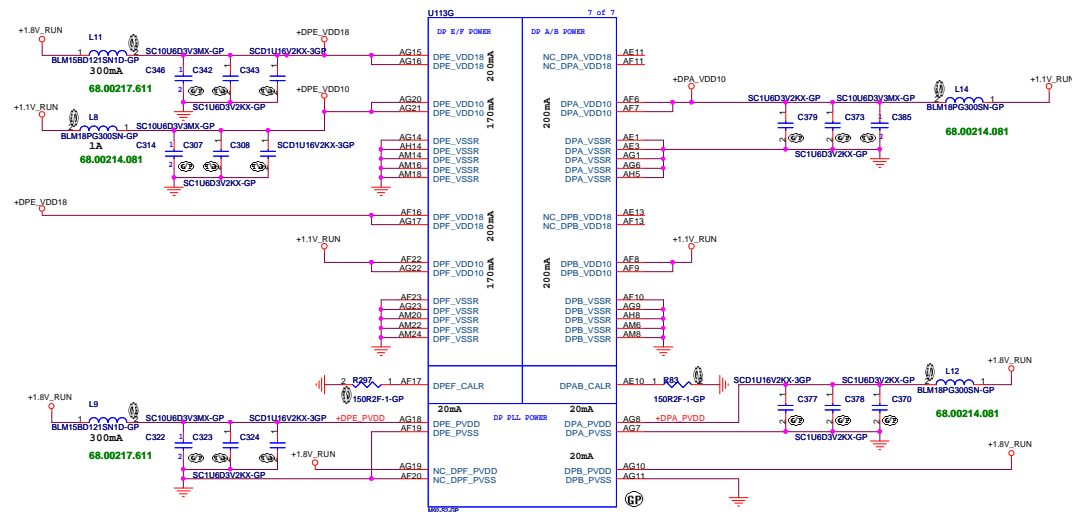
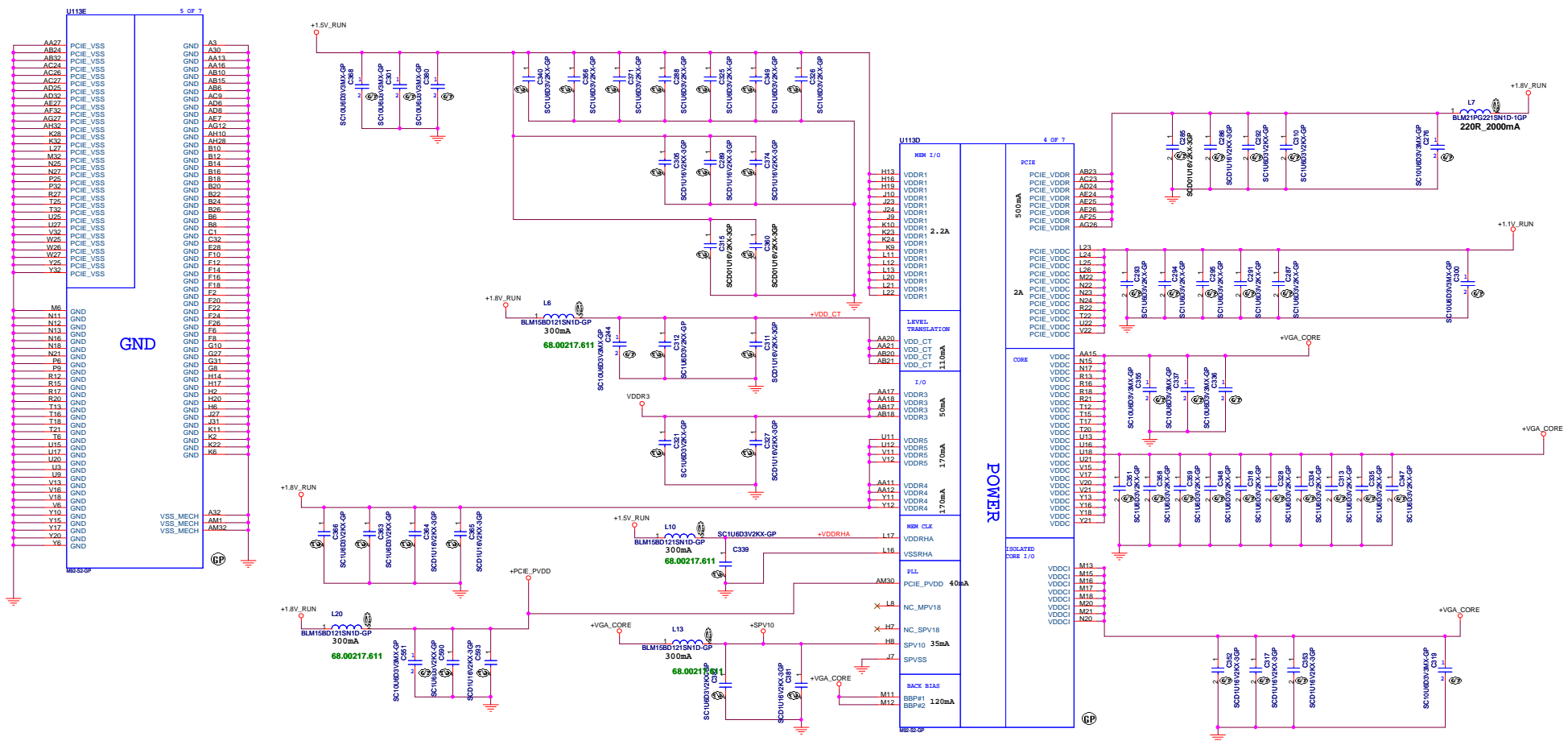
PLACE THESE RESISTORS CLOSE TO
DIFF. PAIRS AND AVOID STUBS TO ALL
DIFF. TRACES.

MINIMIZE THE DISTANCE
BETWEEN THESE RES. AND
100nF AC CAPS

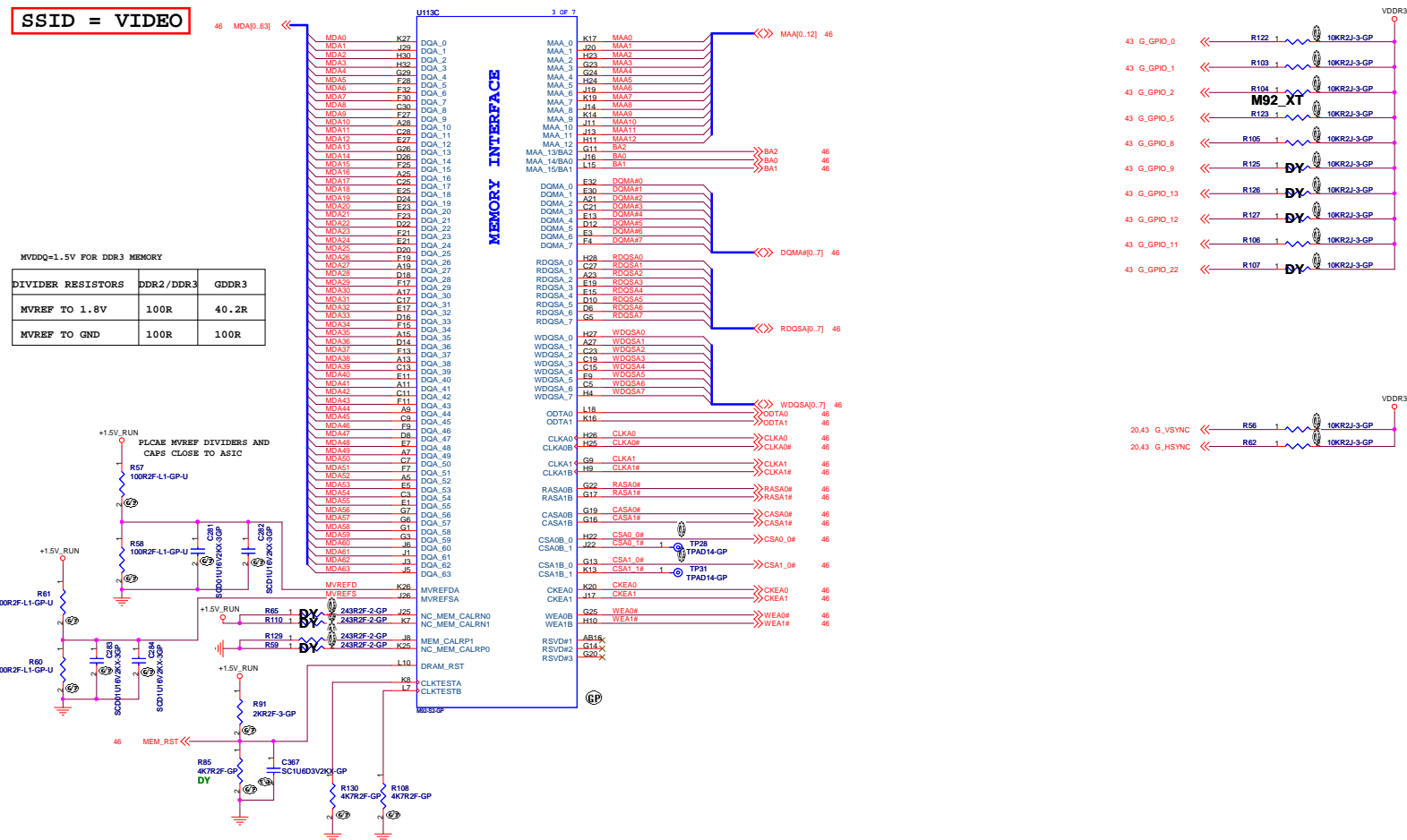


```
H:UMA MODE HDMI PLUG_OUT
L:UMA MODE HDMI PLUG IN
```

SSID = VIDEO



SSID = VIDEO



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESE

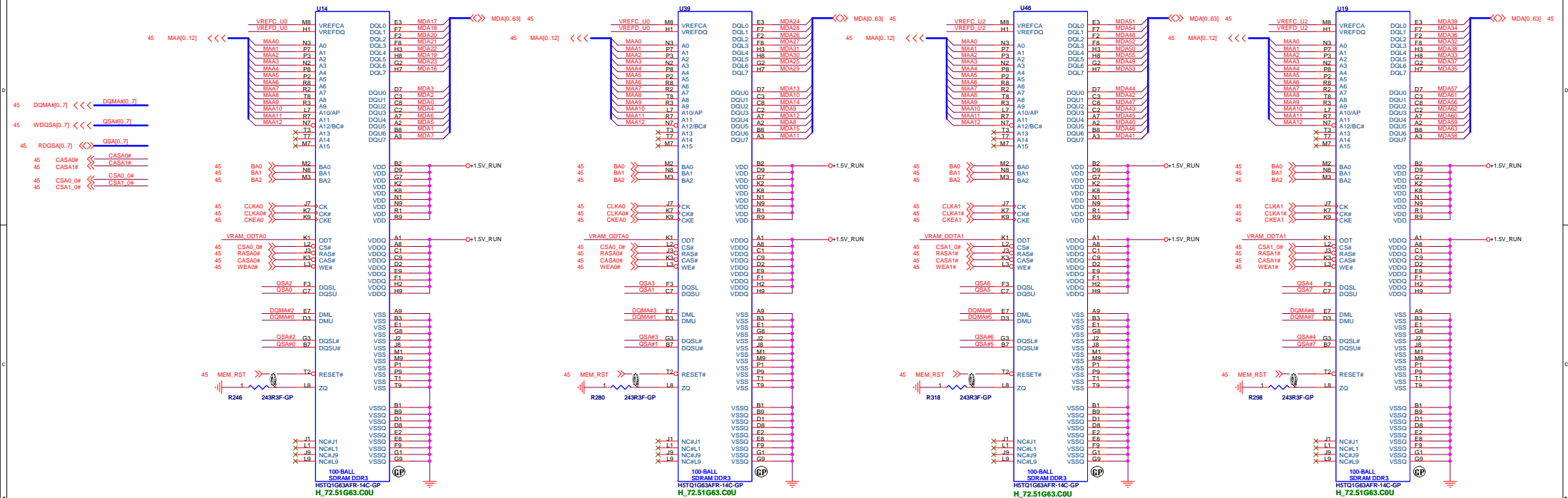
GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0			If BIOS_ROM_EN (GPIO22) = 1			
Size of the primary memory apertures			GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	x000	ST Microelectronics	M25P05A	0100	
	256MB	x001		M25P10A	0101	
	64MB	x010		M25P20	0101	
	32MB	x		M25P40	0101	
	512MB	x	Chingis (formerly PMC)	M25P80	0101	
	1GB	x		Pm25LV512A Pm25LV010A	0100	
	2GB	x			0101	
	4GB	x				

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPI00	Transmitter Power Savings Enable 0= 50% Tx output swing 1 = Full Tx output swing v
TX_DEEMPH_ENB (Internal PD)	GPI01	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1 = Tx de-emphasis enabled v
BIF_GEN2_EN_A	GPI02	v 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPI08	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability v
ROMIDCFG[3:0] (Internal PD)	GPI0[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPI0_22_ROMCSB	Enable external BIOS ROM device v 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI v

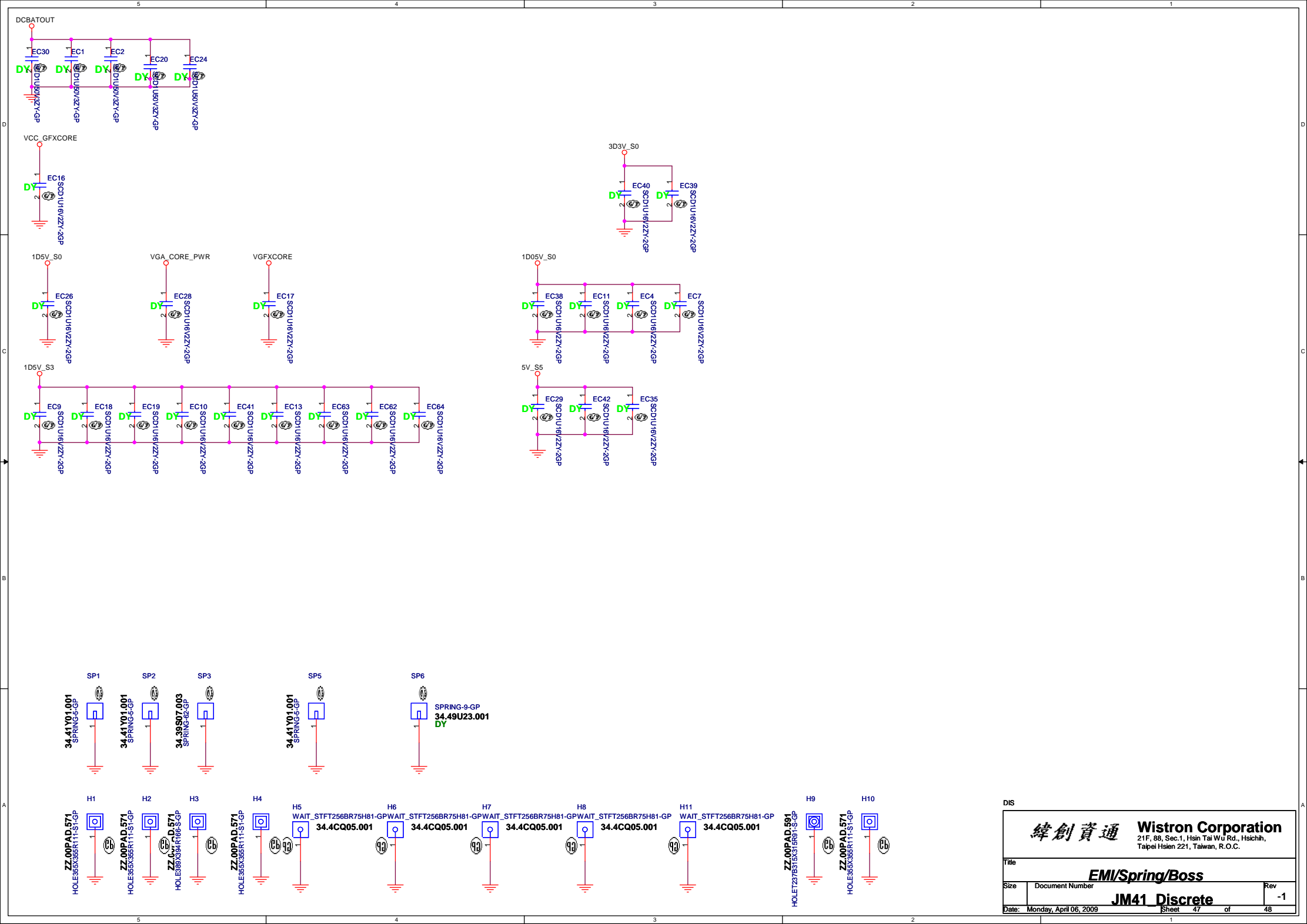
512MB DDR3



Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C





JM41/JM51 DIS Schematic EC Tracking Record

EC #/ Page / Description / Part Affected

EC SC01/11/connect NB1.A31 to GND(For power save)
EC SC02/14/net DIS_EN pull high 10K to 3D3V_S0
EC SC03/20/CN2.pin35 change to AGND
EC SC04/22/R311 change to 39.2K
EC SC05/22/U24.pin2 change to AGND
EC SC06/26/BTB2.pin9 add stand by led control signal
EC SC07/28/U16.pin66 add stand by led control signal
EC SC08/28/add circuit to support green adapter
EC SC09/28/net EJECT_BTN pull high 10K to 3D3V_S0
EC SC10/31/add circuit to stand by led control
EC SC11/40/change GPU power enable signal to ATI_PWR_ON#(low active)
EC SC12/41/change U11 power plane to 1D8V_NB_S0

www.s-manuals.com